DEVELOPMENT AND OPTIMIZATION OF A RECONFIGURABLE TELEMETRY SYSTEM FOR SOUNDING ROCKET PAYLOADS

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DEVELOPMENT AND OPTIMIZATION OF A RECONFIGURABLE TELEMETRY SYSTEM FOR SOUNDING ROCKET PAYLOADS

A

THESIS

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Abstract

This thesis addresses the development of a flight-ready telemetry encoder for the Alaska Student Rocket Project (ASRP) sounding rocket payload. The Frame Oriented eXpandable Integrated circuit Encoder–2007 (FOXIE-07) was developed to resolve crosstalk, timing, and thermal issues in the original FOXIE-03 encoder prototype. A pre-modulation low-pass filter was implemented between the encoder and the FM transmitter to minimize undesired sidebands from the transmitted signal. Complete testing of the FOXIE-07 encoder and pre-modulation filter was performed to certify them as flight-ready components for the SRP5 payload launch from Poker Flat Research Range in 2009.

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CHAPTER - 1

Introduction

1.1. Overview of Alaska Student Rocket Program

The Alaska Student Rocket Program (ASRP) was established at the University of Alaska Fairbanks (UAF) in 1991. The program was developed under the Alaska Space Grant Program with a mission to train students by encouraging scientific research and providing hands-on experience in the design, fabrication and integration of student-built sounding rocket payloads. To date, four successful launches have taken place and the current Student Rocket Project 5 (SRP5) is waiting for launch in winter of 2009.

Figure 1-1 shows a block diagram of the SRP5 communication system. The digital data from the science experiments and the house keeping data are forwarded to the encoder while the analog data are forwarded to the anti-aliasing filter. An anti-aliasing filter is used to filter the higher frequencies in the analog signals before analog-to-digital conversion. The output of the anti-aliasing filter is sent to the encoder where they are combined with the digital signals into a serial data stream. The encoder output is filtered before transferring to the telemetry transmitter for transmission to remove out-of-band emissions. The ground station receives, recovers, stores and displays the data for further analysis. All these components are designed and built by the members of the Alaska Student Rocket Project (ASRP).

1.2. Scope of the Thesis

This thesis addresses the development of a flight-ready telemetry encoder for the SRP5 payload. This work is based on the Frame Oriented eXpandable Integrated circuit Encoder-2003 (FOXIE-03) that was developed by Galen C. Hatfield [1]. The FOXIE-03

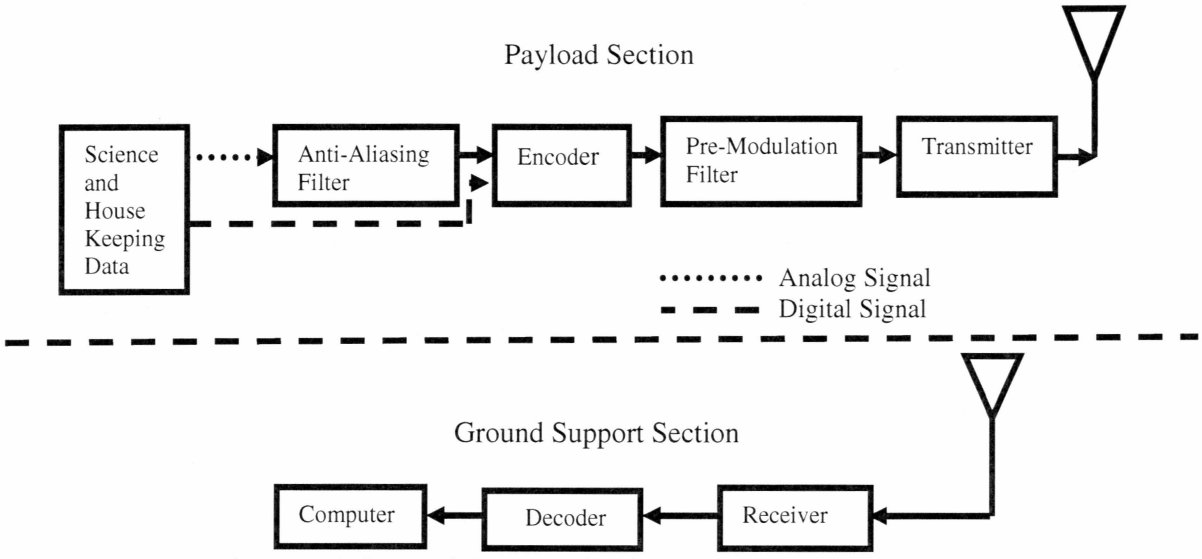


Figure 1-1 General Communication System Block Diagram

prototype provided a successful demonstration of the basic encoder architecture. However, the final FOXIE-03 prototype and documentation left several unresolved issues that needed to be resolved before the FOXIE architecture could be utilized as flight hardware for the SRP5 payload.

The Frame Oriented eXpandable Integrated circuit Encoder–2007 (FOXIE-07) was developed to address the unresolved issues from the FOXIE-03 encoder, and provided a robust, flight-ready encoder for the SRP5 payload. This thesis addresses the following enhancements of the SRP5 telemetry system provided by FOXIE-07:

- Eliminated crosstalk between a few of the analog channels.
- Resolved timing issues for the high speed asynchronous serial channel.
- Addressed thermal issue in the analog-to-digital conversion (ADC) circuit board.
- Designed and implemented a pre-modulation low-pass filter to eliminate the undesired harmonics from the transmission spectrum.

- Enhanced the documentation to facilitate the efficient construction and testing of flight spares.
- Completed acceptance testing of the flight-ready telemetry system.

Detailed explanations of these issues are included in the following chapters.

1.3. Organization of This Thesis

An overview of FOXIE-03 is provided in chapter 2. It highlights the different types of inputs available to the FOXIE encoder and their characteristics. Inputs to the FOXIE encoder includes 64 analog channels, 8 asynchronous serial channels with standard baud rates from 1200 bps to 115.8 kbps and 4 digital channels of 8 bits each. A concise overview about the hardware and firmware implementation of FOXIE-03 is provided within. It also discusses the Inter-Range Instrumentation Group (IRIG) standard data format utilized by FOXIE-03. This chapter concludes with a discussion of the test results on FOXIE-03 and the system limitations leading to the development of FOXIE-07.

Chapter 3 presents the new FOXIE-07 encoder, discussing about the modifications and enhancements made to the firmware and hardware. All the firmware modifications and testing were done using a developmental prototype, that is discussed in this chapter. A new analog board was developed as a part of the developmental process which is discussed in detail. This chapter provides an insight into the improvements made in the FOXIE-07 firmware to overcome the system limitations of FOXIE-03, with particular attention to crosstalk between analog channels and the timing issue in the high speed asynchronous serial channel. A detailed description of the enhancements made to FOXIE-07 by increasing the baud rate of the asynchronous serial channels and ground support data feed is provided. This chapter introduces the software tool developed for configuration of the telemetry data matrix.

Chapter 4 presents the pre-modulation filter required to eliminate spurious radiated signals outside of the assigned radio frequency (RF) signal. This chapter considers the design and layout of the pre-modulation filter. It discusses the tests that validate the performance of the pre-modulation filter in the SPR5 telemetry system.

Chapter 5 is devoted to the testing on FOXIE-07. This chapter gives the detailed descriptions regarding the acceptance test for FOXIE-07 before considering it as flight hardware. Finally, chapter 6 concludes the thesis by highlighting the achievements of FOXIE-07. It also discusses about the possible future upgrades to FOXIE-07.

CHAPTER - 2

FOXIE-03

2.1. Introduction

The SRP5 payload sensors produce different types of data that are encoded and transmitted to the ground receiving station. The encoder prototype for the SRP5 is the Frame Oriented eXpandable Integrated circuit Encoder–2003 (FOXIE-03) designed by Galen C. Hatfield [1]. This chapter gives a brief overview of the inputs, outputs and the internal operations of the FOXIE-03 [1].

2.2. Data Inputs and Channels

The FOXIE-03 has the following inputs:

- 64 Analog Channels - The analog channels are all differential signaling for noise immunity with a range of ± 10 V. Analog-to-Digital converter with an effective sample rate of 400 kilo-samples per second (ksps) and a resolution of 14 bits is used to sample each of the analog channels.
- 4 Digital or Parallel Channels – In a sounding rocket some sensors output signals that can be best represented either as '1'-'0' or 'ON'-'OFF'. To accommodate these signals in the encoder, standard TTL-Level digital ports are implemented. Four digital ports having 8 bits each are developed to process data throughput in excess of 1 Mbps for the parallel channels.
- 8 Asynchronous Serial Channels – A number of the instruments in the SRP5 sounding rocket payload send out data as a serial bit stream. These serial bit streams are not synchronized to the telemetry data stream. Eight half-duplex serial ports are implemented in the FOXIE-03 to process these asynchronous serial data. The asynchronous data streams are merged into the telemetry stream

by the use of a "valid" bit, which indicates the reception of an asynchronous word. The serial data signal must be of the form '8N1' without any parity check. If the start bit is 0 and the stop bit is 1, the word is considered to be valid. To acquire all the valid words, the asynchronous serial channels are sampled 1.1 times the serial baud rate. The word structure of an asynchronous serial word encoded into a standard 16-bit word is shown in Figure 2-1. The asynchronous serial channels have a baud rate of 1200 bps to 115.2 kbps.

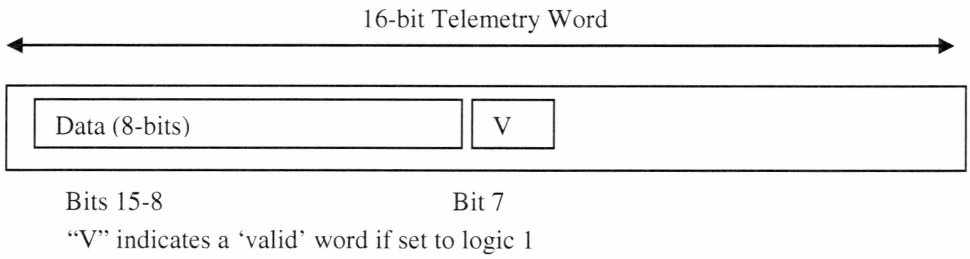


Figure 2-1 Word Structure for Asynchronous serial data [1]

The channels have different sampling rates ranging from 100 sps to 12.7 ksps. A list of all the channels used for SRP5 and their sampling rates are provided in Appendix-A.

2.3. Data Format and Data Output

In general, a payload telemetry system may utilize either a "packetizing" or a "framing" format. In the "packetizing" format, the data packets are transmitted asynchronously one packet at a time with an unspecified time between each packet. Also, the packets are not necessarily uniform in length. In "framing" or "synchronous" format, the data packets are called frames. Frames are uniform in length and continuously transmitted at a uniform rate with no gap between each other.

The Inter-Range Instrumentation Group (IRIG) defines a fixed frame standard for telemetry data formation. For SRP5, a frame format based on IRIG standard 106-05 was adapted to maintain compatibility with the telemetry receiving equipments used by the National Aeronautics and Space Administration (NASA) Sound Rocket Program [2].

Figure 2-2 shows an illustration of a frame based on the IRIG fixed framing format. Each element in the frame is called as "word"; each row is known as "minor frame". A major frame is an integer number of minor frames such that each channel is sampled at least once. S0, S1, S2 and S3 represent channels with different sampling rates. Synchronization (SYNC) and sub-frame identification (SFID) are overheads used for synchronizing the frame with the ground station. A channel having a lower sampling rate may appear once in the frame, whereas one with a higher sampling rate may occur several times.

	Word0	Word1	Word2	Word3	Word4	Word5	Word6	Word7
Minorframe1	SYNC	SFID	S0	S1	S2	S0	S1	S3
Minorframe2	SYNC	SFID	S0		S2	S0		S3
Minorframe3	SYNC	SFID	S0		S2	S0		S3
Minorframe4	SYNC	SFID	S0		S2	S0		S3
Minorframe5	SYNC	SFID	S0		S2	S0		S3
Minorframe6	SYNC	SFID	S0	S1	S2	S0	S1	S3
Minorframe7	SYNC	SFID	S0		S2	S0		S3

Figure 2-2 IRIG Telemetry Standard Data Format

For SRP5, a frame was developed with 32 minor frames and 32 words per minor frame. This frame is called the data matrix. The SRP5 data matrix, together with the channels and their sampling rates, is shown in Appendix-A.

The FOXIE-03 provides the following outputs –

- IRIG standard 106-05 Output – The FOXIE-03 encoder can produce the following types of encoded output signals: Non Return to Zero Level (NRZ-L), Randomized Non-Return to Zero (RNRZ-L), Bi-phase Level and Bi-phase differential. Figure 2-3 shows the output pattern for 'EB90' hex. NRZ-L requires the least bandwidth but with the disadvantage of having long strings of 'zero's' and 'one's' cause problems for the ground support to synchronize with the telemetry stream. A RNZR-L rectifies the synchronization problem by the introduction of a pseudo-random pattern into the telemetry stream. The output considered for SRP5 mission is the "Bi-phase Level" which assure a transition with every bit but requires twice the bandwidth than that of NRZ-L signaling.
- Diagnostics Output – The FOXIE-03 core voltages (±15 V, 5V, 3.3 V), the total current drawn and the internal temperature are monitored and output for diagnostics through the Universal Serial Bus (USB) 2.0 interface.
- Fiber-Optics transmitter – A 1 Hz square wave signal is output through the optical transmitter to be used as a diagnostic signal for the ground support.

2.4. Hardware Implementation

All the different types of inputs could not be implemented on a single circuit board, so four circuit boards are used. In aerospace engineering terminology each circuit board is referred as deck. The FOXIE has four decks. The decks are placed on top of each other in a stack with electrical connections for deck-to-deck communications. Figure 2-4 shows the basic block diagram of FOXIE-03. The bottom deck is the serial board that carries out the conversion from asynchronous serial fiber optics to asynchronous serial data.

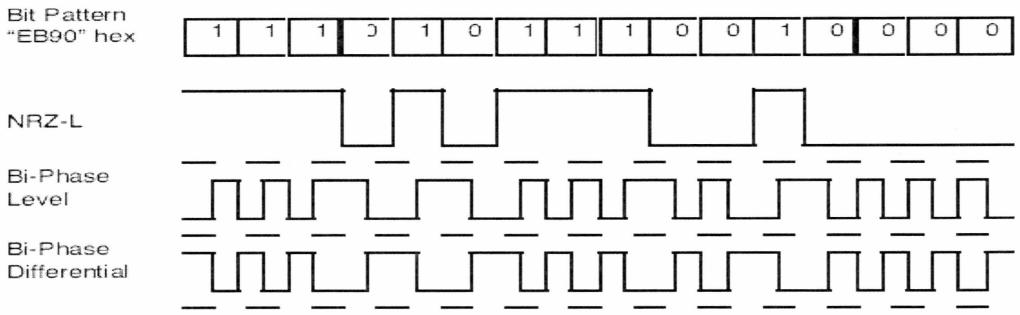


Figure 2-3 FOXIE Output pattern for 'EB90' hex [1]

The second deck is the power board that has the parallel or digital media conversion and the power supply for the FOXIE. The third deck is the core board that provides the brain and heart of FOXIE and controls all operations. It consists of a Cyclone Field Programmable Gate Array (FPGA) from Altera and an MSP430 microcontroller. Finally, the fourth deck is the analog board that controls all the analog inputs. Backplane connectors were used for communicating between the decks. This section gives a brief overview about the hardware design.

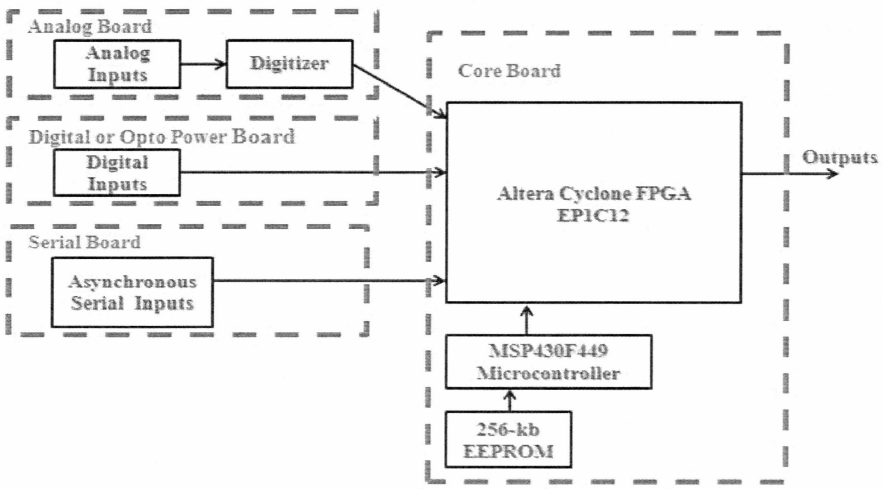


Figure 2-4 Block Diagram of FOXIE-03

2.4.1. Serial Board

The asynchronous serial inputs are half duplex serial fiber optics inputs. The IF-95 fiber optics receiver converts the optical signals to TTL level inputs. These TTL inputs are passed through 74LCX541 octal buffers to the backplane connector. Another octal buffer is used to drive 8 onboard LED's. A red LED indicates no data and a blinking LED indicates data is present on that line.

2.4.2. Parallel and Opto-Power Board

The parallel or digital signals are low speed data that correspond to binary 1 or 0. An example of these data types includes the status input from scientific instruments or digital sensors. The parallel inputs sample the data asynchronously without providing any information to the source when the sample is taken. For high speed data this is not acceptable and a signal called 'strobe' is provided as indication when the sample is taken.

The FOXIE parallel inputs are organized as four ports of 8 bits each. Ports 1, 2 and 3 are asynchronous without any strobe signal, whereas Port 0 works as a high speed asynchronous port with a strobe signal. The other function of the parallel board is to work as the power supply for the FOXIE. There are two options: a) to use the onboard dc-dc converters to generate the required +15 V, -15 V, 5 V and the 3.3 V supply or b) to use the power supply of the SRP5 mission. Jumpers are provided for selecting between these two options – if jumpers on the board are in place then it uses only an external +12 V supply for the dc-dc converters to generate the essential voltages. Regardless of the source of power, monitoring of onboard voltage and current are provided. The four bus voltages are monitored by voltage dividers and total current drawn is monitored by a magnetic sensor. All these monitored data and the digital data from the parallel channel are passed to the core board through the backplane connector.

2.4.3. Core Board

The core board is a crucial component in FOXIE consisting of the Cyclone FPGA and MSP430 microcontroller. The main function of this board is to gather all the information from the other boards according to the data matrix and produce an encoded output. It consists of many components, but the most basic component is an EEPROM – Atmel AT25256A. The EEPROM is burned with the SRP5 data matrix. The EEPROM is followed by the MSP430 microcontroller – MSP430F449 from Texas Instruments. The microcontroller has a vital role to play – at start up it configures the FPGA with the data matrix. It also processes the voltage, current and temperature information of the FOXIE as a diagnostic output through the Universal Serial Bus (USB) interface. Another diagnostic output is provided through the Industrial Fiber-Optics IF97 transmitter. This signal is compatible with the IF95 receivers and provides a diagnostic link to the SRP5 umbilical interface. It is a half duplex 1200 baud rate signal corresponding to the character "U".

The FPGA chosen is a Cyclone EPC12Q240 FPGA from Altera, which has 240 pins on a Plastic Quad Flat Pack (PQFP) package. It has 12,060 Logic Cells (LC), 240 kbits of SRAM and 2 Phase Lock Loops (PLL). The LC and the PLL of the chip requires a +1.5 V, whereas the input/output banks work on +3.3 V. Altera recommends using separate planes for the power supply, ground and input/outputs. Thus the core board has 8-layers. Cyclone FPGA is Static Random Access Memory (SRAM) type and can be configured by three ways on start up – Active Serial, Passive Serial or using a JTAG. The core uses board two types of configuration modes – Active Serial and JTAG. For configuring it in Active Serial mode – Altera provide low cost configuration devices like EPCS1, EPCS4 or EPCS16. The core board uses an EPCS4 configuration device. Two headers are provided. One can be used for JTAG configuration and the other for Active Serial configuration using the EPCS4. Two oscillators operating at 48 MHz and 18.43 MHz, respectively, are used as the clock source for the Cyclone. The encoded output from EPC12Q240 is buffered by using a 74LCX541 chip. In addition, the outputs are also

buffered using an LM6144 op-amp. LM6144 has a 17 MHz bandwidth and acts as a low-pass filter for the telemetry outputs. The output impedance is 75 Ω having a signal level of 3.3 Vp-p with a zero level of 1.5 V. Eight diagnostic LEDs are used for providing onboard diagnostics and run time display.

2.4.4. Analog Board

The Analog-to-Digital Converter (ADC) used for the analog board is the AD7899 from Analog Devices. It is a low power, single-ended input 14-bit Successive-approximation-register (SAR) ADC with an input range of ± 10 V. Since the FOXIE-03 has 64 channels, analog multiplexers are used to merge the 64 channels into a single channel sampled by one ADC. Eight 16:1 ADG406 multiplexers, serve this purpose. The analog channels are connected to the board as twisted pair differential inputs, which are physically wired to the 62-pin high density D-SUB connectors.

2.5. Firmware Implementation

The Cyclone FPGA controls all the functions of the encoder, which is configured with the data matrix on startup by the MSP430 microcontroller. At start up, the microcontroller loads the FPGA with the data matrix and the special function registers. It also samples the voltage, current and temperature reading every 57.5 msec and forwards it to the USB to be displayed in the user computer.

Figure 2-5 shows the block diagram for the FPGA firmware. The Clock Core provides the clock needed for all the functions inside the FPGA, a 96 MHz clock is used as master clock for this synchronous design. The master clock is generated by using the inbuilt PLL of the Cyclone that works on the external 48 MHz oscillator. The main clock is selected based on the least common multiple of the required bit rates. Another 18.43 MHz oscillator is used to generate all the required baud rates for the serial channels. The

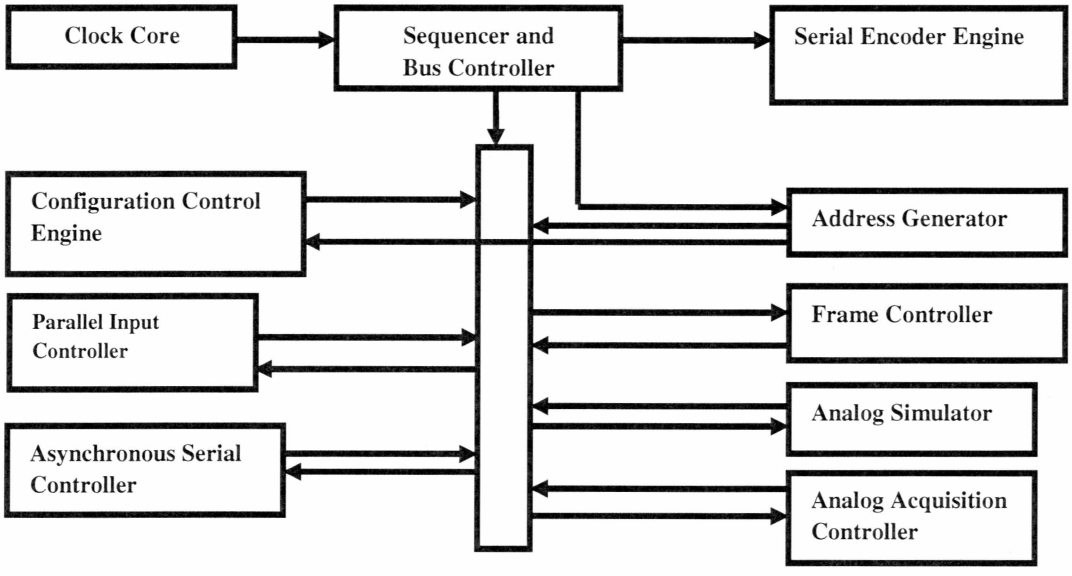


Figure 2-5 Block Diagram of FPGA Firmware

Configuration Control Engine stores the data matrix and the special function registers uploaded by the MSP430 microcontroller. The Serial Encoder Engine initiates the encoding on receiving the load word from the Clock Core. On the rising edge of the bit-clock from Clock Core the Serial Encoder Engine loads the word from the Sequencer block and starts encoding. At the same time the Address Generator block is updated to the next address. The internal bus read cycle is selected one bit-clock later and the Sequencer block loads the next word specified by the data matrix into the transmit buffer located in the Sequencer block. The selected addressed station loads its data on the tri-state internal bus. The Sequencer goes idle for 12 bit-clock cycles and begins the encoding process again. All the blocks have specific functions to perform during the encoding cycle. The Frame Controller generates the SFID word for the data matrix and works as a frame counter. The Analog Simulator is used to generate a 1 Hz triangular waveform for simulating the analog inputs. The Parallel Input Controller takes care of the parallel data input. Asynchronous serial data is taken care of by the Asynchronous Serial Controller sampling the data at 1.1 times the required baud rate. The Analog

Acquisition Controller controls the analog data. It uses the sample-on-demand architecture. It begins with the previous data for that channel being read from the sample memory. During that time, a conversion signal is sent to the ADC for sampling the channel requested. The sample data are stored in the memory to be used for the next read cycle.

2.6. Test Results

Extensive testing of all the serial, analog and parallel channels were done by ASRP members as per the testing procedure provided [1]. It was observed that the high speed analog channels having a sampling rate of 2 ksps and 1 ksps have crosstalk that affected some low speed analog channels as well. Also, the 115.2 kbps baud serial channel partially failed the loop back tests. A summary of the test results are provided in Appendix-B.

2.7. System Limitations

The following system limitations were observed after the FOXIE-03 was delivered to the members of ASRP.

- Crosstalk in channels – The test results of FOXIE-03 indicated crosstalk in numerous channels, especially the high speed analog channels. This crosstalk caused non-functionality of the high speed channels.
- Analog Board – Although the analog board was functional, it was found that one of the multiplexer chips operated at excessive high temperature.
- Asynchronous Serial Channel – The high speed asynchronous serial channel having a baud rate of 115.2 kbps partially failed the loop back test.
- Ground Support Data Feed – The ground support of SRP5 requires monitoring the status of all the channels at ground station that was not implemented in FOXIE-03.

- Flight Hardware – ASRP requires flight spares of all its instruments for a particular mission. Duplicate flight hardware for FOXIE-03 was not provided.
- Pre-Modulation filter – The pre-modulation filter required to limit the bandwidth of the telemetry stream was not implemented.

CHAPTER - 3

The FOXIE-07 Telemetry Encoder

3.1. Introduction

The FOXIE-03 prototype encoder was successful in demonstrating the basic functionality required for the SRP5 payload. However, the unresolved timing issues required continued development to meet all of the SRP5 requirements. The FOXIE-07 encoder presented in this thesis was developed using the basic hardware and firmware of the FOXIE-03 encoder, with the following changes to fix the major problems with FOXIE-03:

- Redesign of the analog board to resolve the heating issue.
- FPGA firmware modifications to remove the glitches that were responsible for crosstalk and timing issues in the high speed analog and serial channels.

The FOXIE-07 encoder also includes the following new capabilities:

- The MSP430 firmware was modified to improve the communication protocol.
- The maximum baud rate for the asynchronous serial channels was increased by changing the clock.
- A configuration tool was developed to facilitate future changes in the data matrix.
- A serial output connection to the ground support equipment (GSE) was added for improved diagnosis and monitoring of the payload before launch.

3.2. Developmental Prototype for FOXIE-07

The following resources from the FOXIE-03 project were available to begin the development of the FOXIE-07:

- OrCAD schematic files for all the boards.
- OrCAD layout files for the all the boards except the analog board.
- Core board PCB (Printed Circuit Board) with a few damaged pads for the MSP430.
- MSP430 and FPGA firmware files.
- TACOS (Telemetry Automatic Configuration and Operations Software) monitor software files used to display the voltage and current output from USB2.0.

The FOXIE-03 was considered as flight hardware in view of the fact that it successfully demonstrated the encoder functionality other than crosstalk in few of its channels. So it was decided not to lay a hand on FOXIE-03 and its hardware for any sort of firmware or hardware modifications. As a result, a new developmental prototype for FOXIE-07 was built with the available resources and development of the missing resources:

- Analog board – the layout for the analog board was created and a new analog board was developed.
- Core board – the Cyclone FPGA, MSP430 and EEPROM chips were successfully mounted on the damaged core board with the help of the Electrical Design & Analysis Lab of UAF. This repaired 8-layer board was used for development & testing of FOXIE-07 and new boards were ordered and assembled for flight hardware. Figure 3-1 shows the core board with wires used to connect pins where pads were removed.
- Serial and Power board – new boards were fabricated based on the FOXIE-03 design and layout documentation.

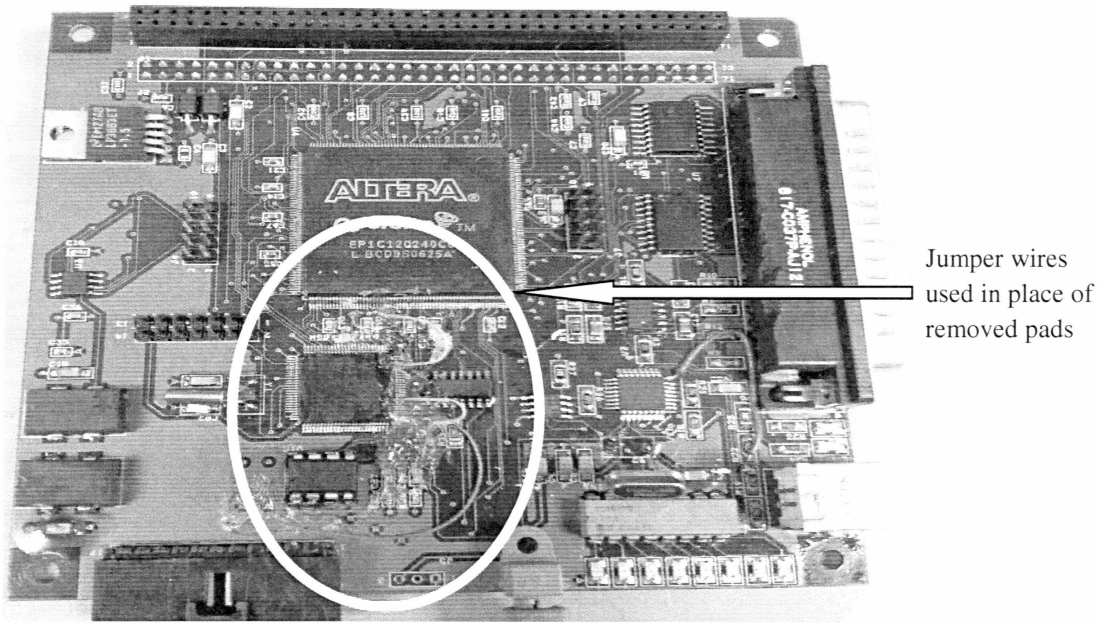


Figure 3-1 Core Board with jumper wires for damaged pads

3.3. Redesign of the Analog Board

The FOXIE-03 analog board has a mysterious heating issue with one of the multiplexers. This heating is only related to the specific multiplexer position, shown in Figure 3-2. It was found that the heating of the multiplexer continues even after replacing the multiplexer chip. While the abnormal heating was cause for concern, it did not appear to disrupt the performance of the analog board. So it was decided not to stress that analog board through further testing. A new analog board with an improved layout was designed and fabricated for FOXIE-07.

The analog board for FOXIE-07 follows the same design as for FOXIE-03. The 14-bit resolution AD7899 from Analog Devices was used as the ADC for the analog board, which was combined with AD817 and AD818 instrumentation amplifiers to realize the sample-on-demand architecture. Eight ADG406 16:1 multiplexers from Analog Devices

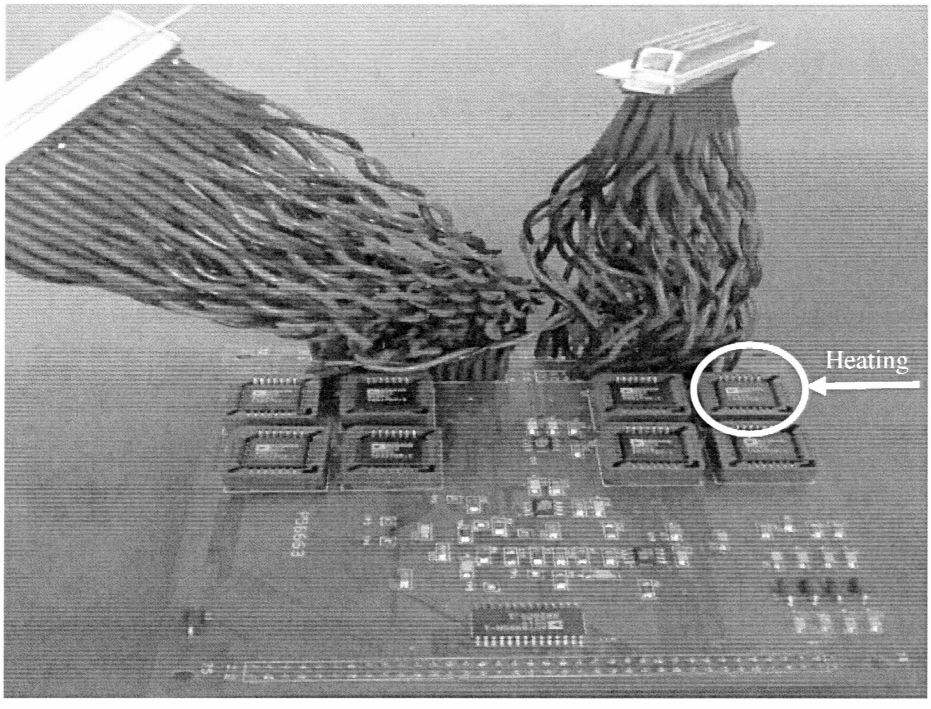


Figure 3-2 Analog Board for FOXIE-03

were used to merge the 64 differential analog channels down to one channel sampled by the single AD7899. Passive L-C type filters were used for power conditioning of the supply voltages. The only modification done in the new board was the replacement of four 32-pin DB connectors with two 62-pin High Definition DB 62 connectors. The replacement was done to reduce noise by receiving the differential analog signals on the PCB, thereby reducing the length of the needed differential pair wires. It also reduces the complexity in building the hardware. Once the schematic was completed, the next step was to layout the board using computer aided design (CAD) program called OrCAD Layout Plus. The three steps followed for layout were placing, routing and finishing. All the components chosen were SMD (Surface Mount Devices) type except the ADG406, which was 28-pin PLCC (Plastic Leaded Chip Carrier) type. Keeping in terms with the other boards of FOXIE, the size of the analog board was maintained at 4720 mils by

4720 mils. The first component to be placed was the backplane connector, which was positioned at 4400 mils by 574 mils relative to the board lower left corner. This was followed by the placement of the two DB 62 connectors according to the requirement of the SRP5 payload. The wiring harness of the payload required that the two connectors to be placed at 180 and 270 degrees with respect to the back place connector. The AD7899 was then placed adjacent to the back plane connector to reduce the length of the digital signals. The ADG406 multiplexers were placed to maintain almost the same trace length for both the positive and negative channels to reduce eddy currents in the differential channels. The other components were placed to minimize connection length, thereby reducing noise and interference in the digital lines. The bypass capacitors and feedback registers were placed near to the ADC and instrumentation amplifiers.

The next step was to route the board. The signal trace widths were chosen to be 6 mils. The ground and power trace widths were chosen to be 12 mils each. The trace-to-trace spacing was 6 mils and the via-to-via spacing was 12 mils. It was also desirable to have all the digital lines at the top layer without any crossover with analog lines. When all the rules are set, the ground and power lines were routed manually. While routing the power signals, care was taken not to route supply lines below the ADC to reduce noise in the ADC. However, ground signals were allowed to pass under the ADC. OrCAD Smart Route utility was used to route all the differential signals. The feedback signals were made to pass below the instrumentation amplifier, as recommended by the data sheets. After the completion of routing, the cleanup design command was executed to reduce the traces to the shortest possible length. Figure 3-3 shows a routed analog board. Finally the ground plane and solder mask were applied on the top and bottom layers of the 2-layer board.

The fabricated analog board is shown in Figure 3-4. Testing of this new analog board verified that the multiplexer heating issue in the FOXIE-03 analog board was not present in this new design.

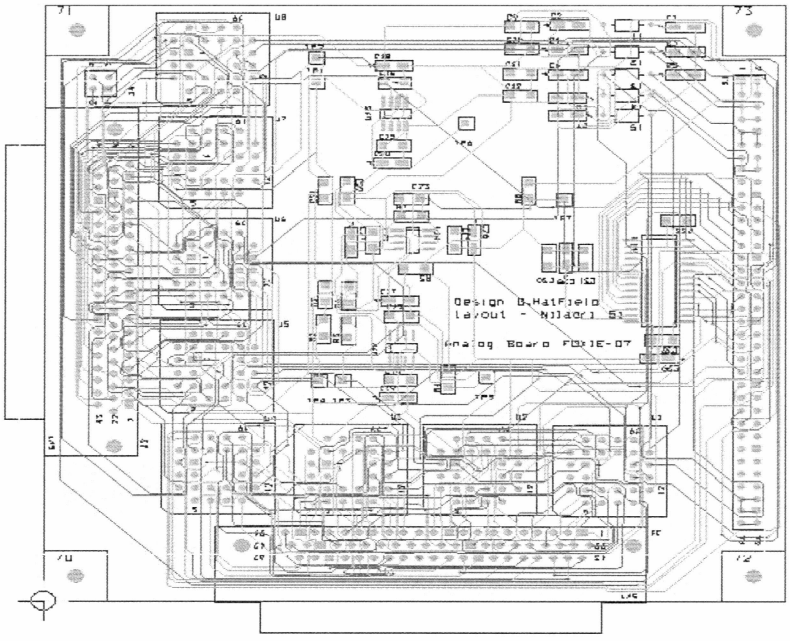


Figure 3-3 Routed Analog Board for FOXIE-07

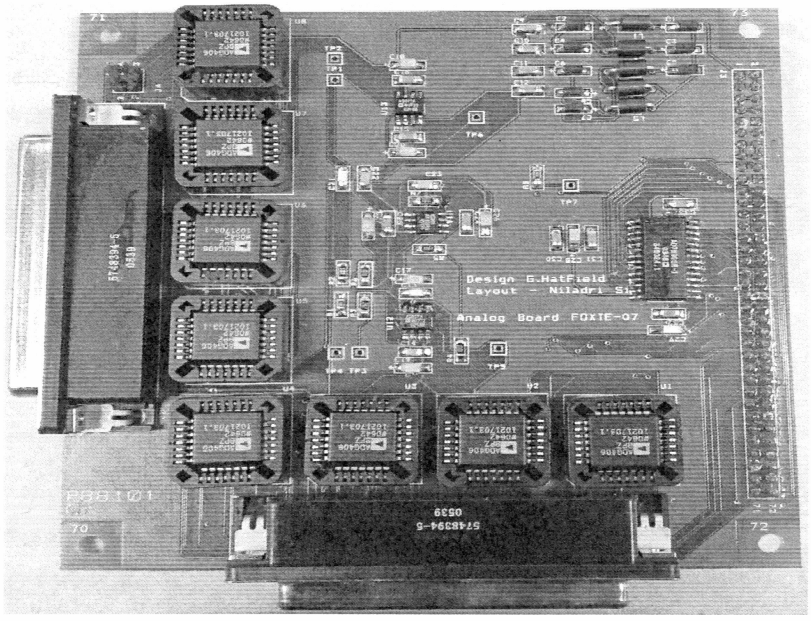


Figure 3-4 PCB for the Analog Board

3.4. FPGA Firmware Modifications

The design of the FOXIE encoder was entirely based on created IP (Intellectual Property) functions. The block diagram environment of Quartus II software from Altera was used to create the IP functions using Very High-speed integrated circuit Hardware Description Language (VHDL)-based mega-functions to reduce design time and simplify troubleshooting [3]. All of the IP functions from FOXIE-03 firmware were individually compiled to understand their design logic and input/outputs requirements, as given in the block diagram of Figure 3-5. Each block in the diagram represents an IP function and the role of each is explained in section 2.5. All these IP functions were linked together to create the top level entity tm4nexys, the encoder engine. The top level entity was compiled without any error. The output signals of the top level entity tm4nexys were observed using a Mixed Signal Oscilloscope, which reveals glitches in the NRZ and Bit-Clock signals, shown in Figure 3-6.

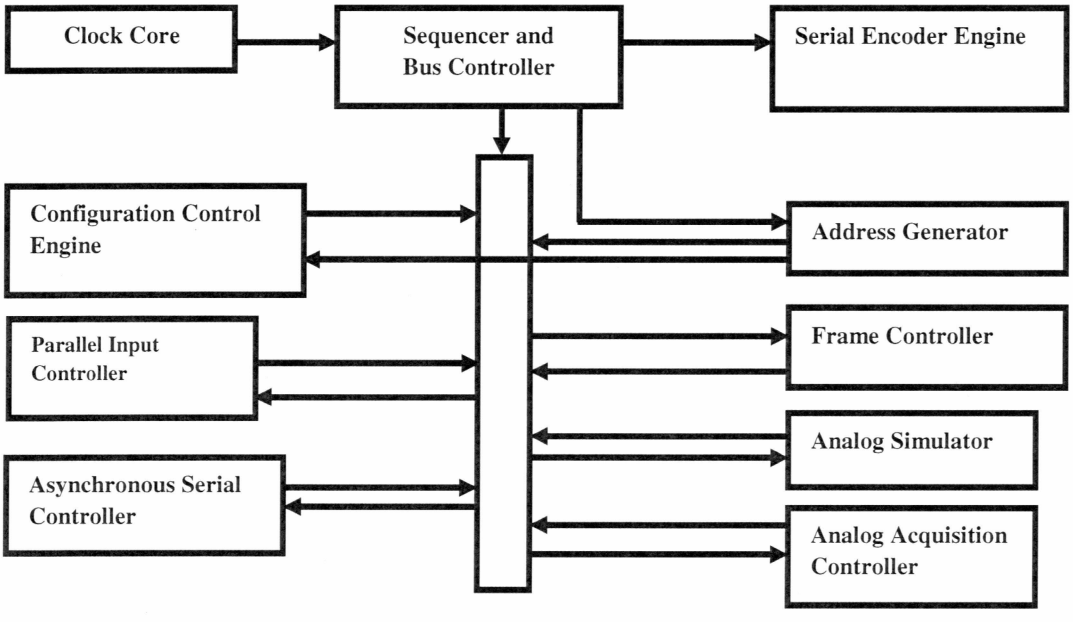


Figure 3-5 Block Diagram of FOXIE Firmware

Figure 3-6 Glitches in Bit-clock and NRZ outputs from the TM encoder engine

The FOXIE design is based on the synchronous design principle, in which a single clock signal triggers all events. A synchronous design behaves in a predictable manner as long as the timing requirements for each register are met. The data inputs to the registers are usually sampled and transferred to the outputs during the rising edge of the clock. Changes happening on the data inputs do not affect the value of their outputs until the next active clock edge. Since the internal circuitry of the registers isolates the data inputs from outputs, instability in the combinational logic does not affect the intended operation of the design as long as the following timing requirements are met [4]:

- Before an active clock edge, the data input is settled for at least the setup time of the register.
- After an active clock edge, the data input remains stable for at least the hold time of the register.

If either the setup or hold time of a register is violated, the output can be an intermediate voltage between the high and low levels, known as metastable state. This state is not stable and can cause small perturbations or glitches in the signals.

To remove the glitches from the output of the top level entity, all the IP functions were analyzed. This revealed the use of clock latencies within the comparators in tm3addrgen IP function and in the decoder of tm3seq IP function, as shown in Figure 3-7 and 3-8. Clock latencies were used to delay the occurrence of the output after the specified clock

pulses. These latencies might have been introduced in the prototype to meet the timing requirement of the design, but ultimately were responsible for the glitches in the output.

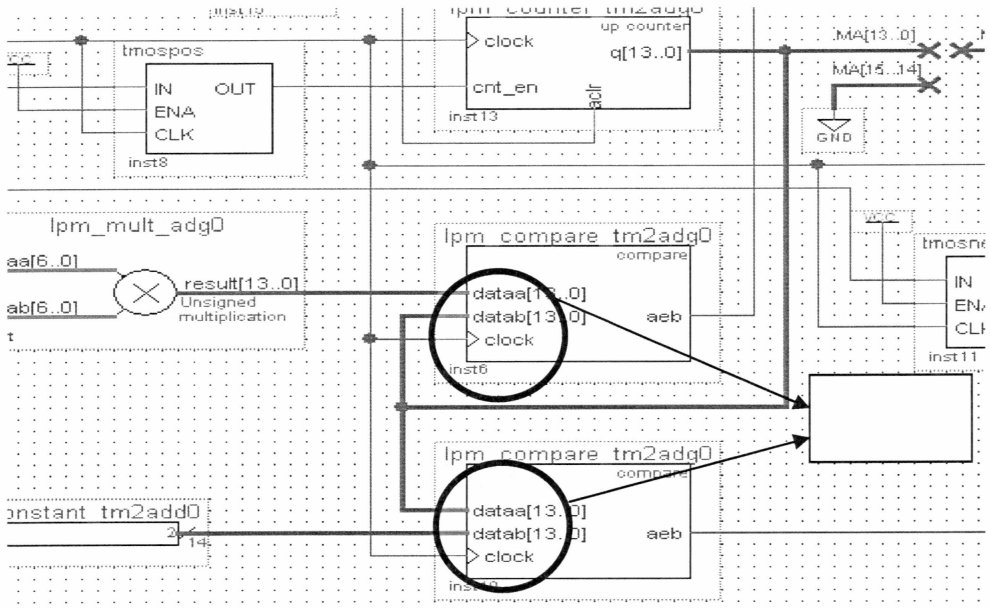


Figure 3-7 The tm3addgen IP function for FOXIE-03

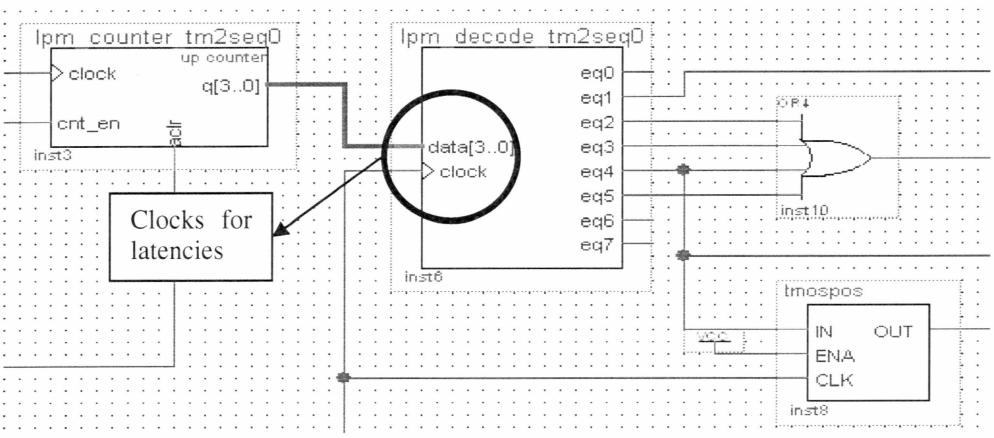


Figure 3-8 The tm3seq IP function for FOXIE-03

The tm3addrgen IP function corresponds to the Address Generator block in the block diagram of Figure 3-5. The Address Generator block generates the hexadecimal addresses for the analog, serial and parallel channels. Figure 3-9 shows the block diagram of the Address Generator block. The Address counter generating all the addresses was controlled by the comparators. The comparators generate a signal to clear the counter as soon as the address equals the size of the data matrix. These comparators have clock latencies in them, which were undesired because it is logical to clear the address counter as soon as it equals to the last address of the data matrix rather than after a delay of few clock pulses. Accordingly, the latencies were removed.

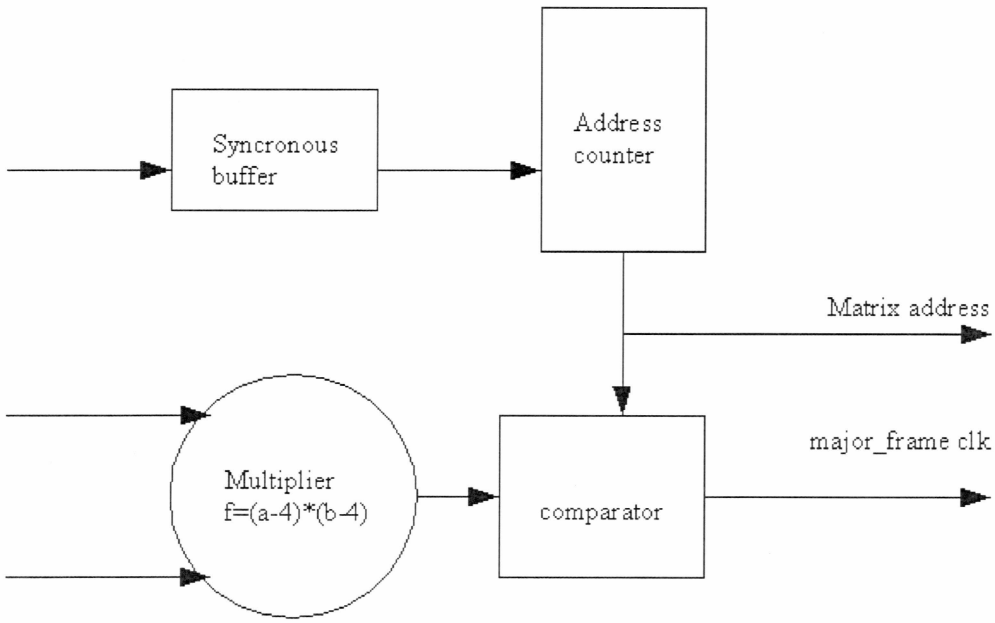


Figure 3-9 Block Diagram of Address Generator [1]

The tm3seq IP function corresponds to the Sequencer and Bus Controller block in the block diagram of Figure 3-5. The Sequencer and Bus Controller control the data bus as

well as the sequence of operations before data is encoded. The block diagram for the Sequencer and Bus Controller block is shown in Figure 3-10. The sequencer is implemented as a 4-bit ring counter. The counter is updated on the rising edge of the bit-clock from the Clock Core. The rising edge of the load word resets the counter. "The first cycle provides the "upd-addr" signal to the address generator. The next cycle asserts the RD-REQ and the remaining cycles are idle" [1]. Clock latencies were used on the decoder generating the upd-addr and RD-REQ signal. It was decided to removes those latencies in the upd-addr signal, which introduced unnecessary delays of 8-bit clock pulses in the update signal to the address generator.

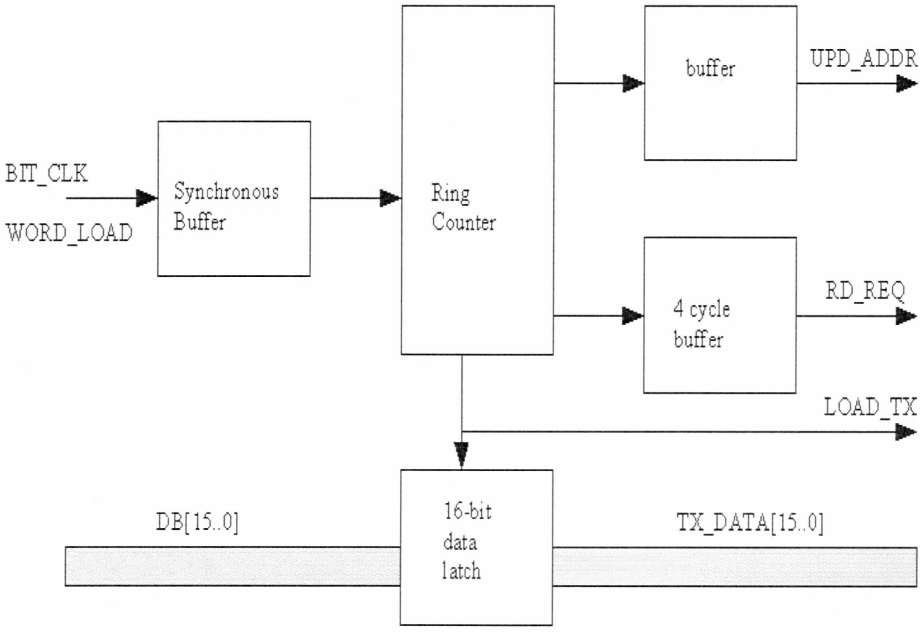


Figure 3-10 Block Diagram of Sequencer and Bus Controller [1]

Once these clock latencies were removed, the top level entity tm4nexys was compiled using Quartus II. Timing analysis during compilation reported that the timing

requirement could not be achieved along 1,978 paths in the chip. The top level entity was again analyzed using Design Assistant from Quartus II software. Design Assistant highlights many warnings in the tlop level entity due to combinational loops, asynchronous clock domain, and non – synchronous design structure. These small warnings can be harmful if ignored. Oscillatory behavior in the output waveform can occur because of combinational loops in the logic design. A simple example of combinational loop is shown in Figure 3-11. A NAND gate input is fed with its output. Figure 3-12 shows the oscillatory output of combinational loop. Combinational loop behavior generally depends on the relative propagation delay through the logic involved in the loop. The propagation delays can change, which means the behavior of the loop is unpredictable.

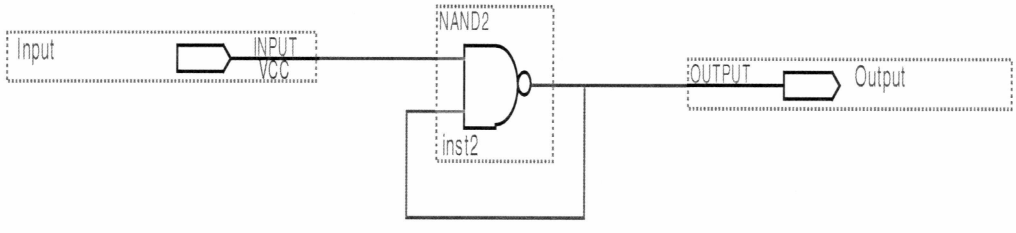


Figure 3-11 Example of Combinational Loop

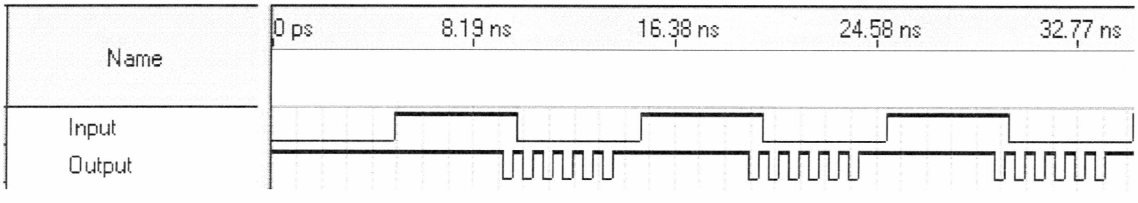


Figure 3-12 Oscillatory behavior of the output waveform due to combinational loop

Altera in Cyclone Handbook recommends using registers to remove combination loop warnings and also using registers in front of asynchronous inputs to remove asynchronous clock domain warnings [4]. Figure 3-13 illustrates the use of a register to remove the combinational loop errors in the output signal of the above example. The D-flip flop uses a clock signal of 5 nsec to ensure the propagation delay is met. Figure 3-14 shows the output waveforms. For the FOXIE firmware, the timing requirement for the design was met once the recommended registers (D-flip-flop) for both combinational loops and asynchronous inputs were added to the IP functions. The output signals of the top level entity tm4nexys were again observed and the glitches were absent from the NRZ and Bit-Clock output, as shown in Figure 3-15.

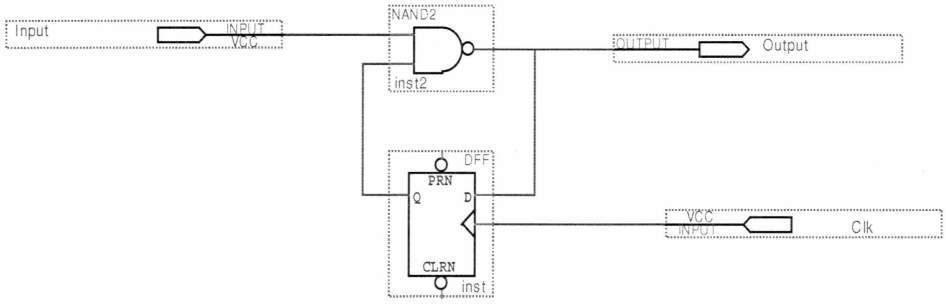


Figure 3-13 Register to remove Combinational Loop Error

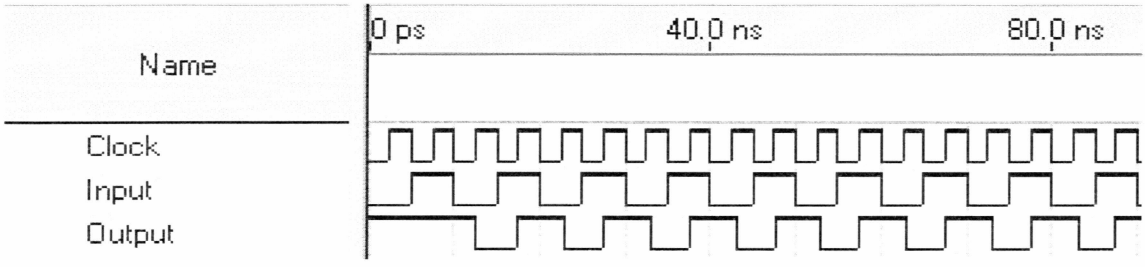


Figure 3-14 Output waveform without oscillations

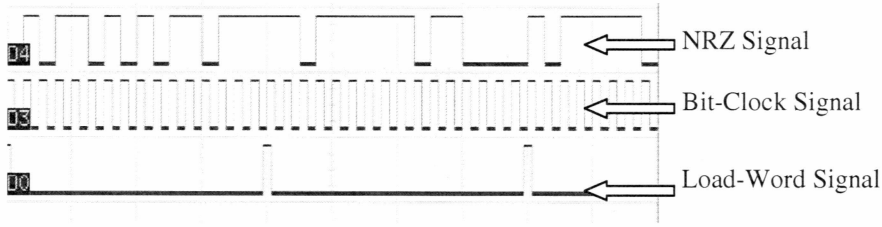


Figure 3-15 Signals without Glitches

After these modifications the encoder core was operated without any glitches in the output signals. But while testing the analog channels, it was still observed that the higher sampling rate channels overlapped into the next channel in the data matrix. For example, ACH17 overlaps over ACH18 and ACH16 overlaps to ACH17, as shown in Figure 3-16. This overlap was not observed in lower sample rate channels.

: TM Data Structure (the PCM Matrix)

3	4	5	6	7	8
ACH16	ACH17	ACH18	S0	S1	S2
ACH16	ACH17	ACH18	S0	S1	S2
ACH16	ACH17	ACH18	S0	S1	S2
ACH16	ACH17	ACH18	S0	S1	S2
ACH16	ACH17	ACH18	S0	S1	S2
ACH16	ACH17	ACH18	S0	S1	S2
ACH16	ACH17	ACH18	S0	S1	S2

Figure 3-16 FOXIE-07 data matrix

The tm4aaqc IP function corresponds to the Analog Acquisition Controller block controlling all the analog channels. This block was scrutinized in detail to identify and

solve the crosstalk problem. The block diagram of the Analog Acquisition Controller block is shown in Figure 3-17. The Analog Acquisition Controller implements a sample-on-demand type of data acquisition. This means that a channel being requested reads the previous data from the memory while also storing the new sampled data from the ADC into the memory. "On the rising of RD-REQ (if an analog channel is chosen) the address is corrected (by subtracting the base address from it) and passed to the analog multiplexers to enable the proper channel" [1]. The ADC conversion is started by NANDing the TX_LOAD and the results of the bit comparator. The converted data is stored into memory to be fed into the tri-state data bus. The tri-state data bus is enabled by ANDing the RD-REQ and the mux_latch output from the bit comparator.

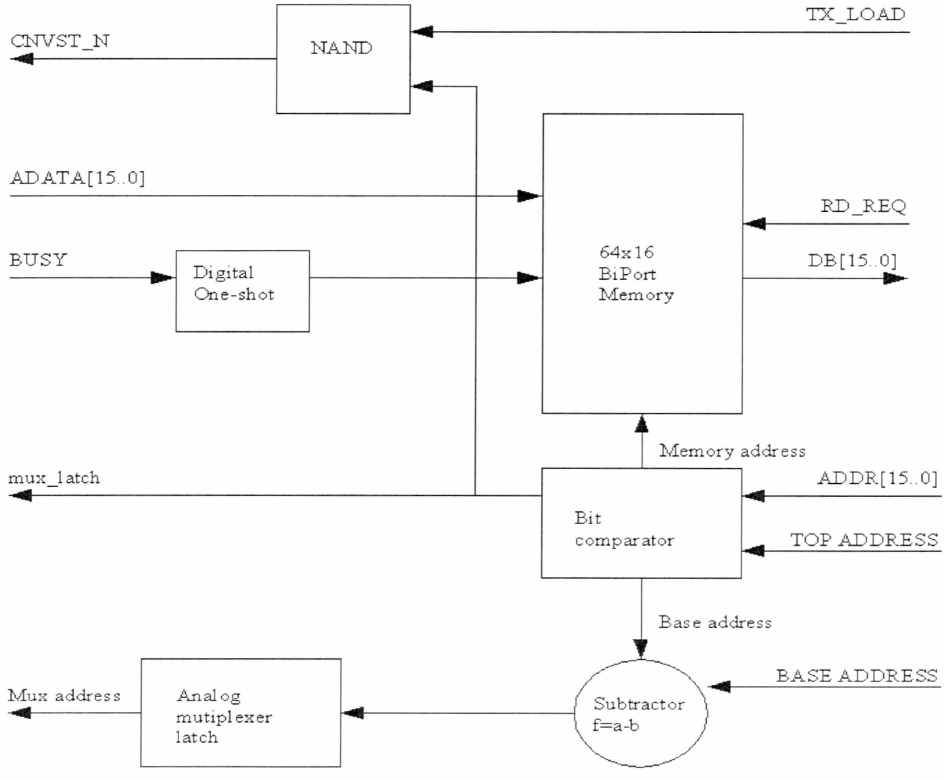


Figure 3-17 Block Diagram of Analog Acquisition Controller [1]

A Mixed Signal Oscilloscope was used to observe all the signal outputs from the tm4aaqc IP functions. It was found that the enable signal for the tri-state data bus has glitches, as shown in Figure 3-18. These glitches in the enable signal might be responsible for enabling the tri-state data bus and sending unwanted data from the stored memory into the data bus, causing the overlap of data for the high speed analog channels.

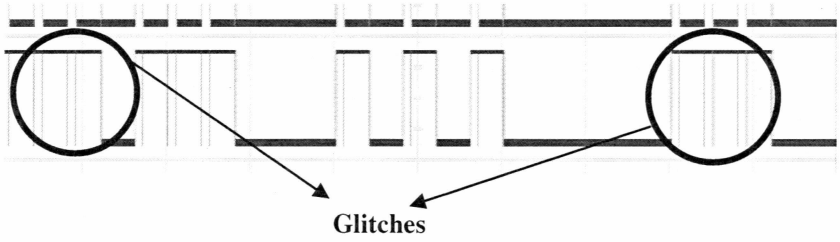


Figure 3-18 Glitches in Enable Signal for Tri-State Data Bus

The problem was solved by extending the pulse width of the RD-REQ signal by 30.9 nsec to ensure meeting the setup and hold times for all the registers. Figure 3-19 shows the tri-state data bus enable signal once the RD-REQ pulse width is extended by 30.9 nsec. Subsequent testing of the analog channels verified the removal of crosstalk and timing issues in the analog channels.

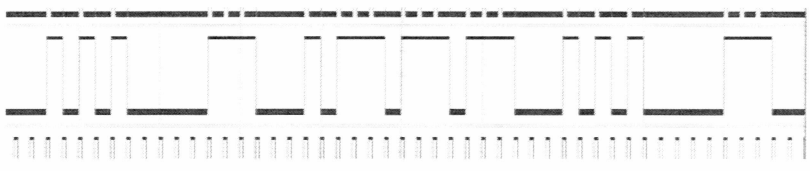


Figure 3-19 Enable Signal for Tri-State Data Bus

A simple loop back test was used to test the asynchronous serial channels, which is described in Chapter 5. The aim of the loop back test was to send encoded serialized data to the decoder where they are re-serialized and compared with the original data to determine if errors had occurred. If a match exists, it verifies the data is received correctly. The WinSSD software transmits 64 times the pattern "55AA" followed by 20 times the phrase "The quick brown fox jumped over the lazy dog's back". All the serial channels passed the test except the serial channel with the maximum baud rate of 115.2 kbps, which failed to pass the long phrase.

The block diagram of the Asynchronous Serial Controller is shown in Figure 3-20. It receives and decodes the asynchronous data from the serial channels. A clock signal that is 16 times the baud clock is applied to the state machine. The falling edge of serial-in signal starts the state machine. After 158 baud clock cycles the state machine goes into the idle state until the next falling edge on the serial-in signal. Samples of the serial-in signals are taken and clocked into a shift register every 16 baud clock cycles. The serial word is sampled on the 157^{th} cycle and the validity of the received word is evaluated. A word is valid if the start bit is 0 and stop bit is 1. If the signal word is valid, the valid bit is set. The received data is latched to be interfaced with the internal tri-state data bus. The valid bit is cleared with each read cycle.

The asynchronous serial channel loop back test was analyzed for FOXIE-03 [1]. It was found that at random intervals, two valid words would be encoded when only one was sent causing fatal errors in serial loop back test. The problem was solved by extending the width of the valid bit reset pulse to 20.8 nsec, to ensure meeting the setup and hold time for the register which stores the 'valid' bit. Although the solution was implemented for FOXIE-03, still the high speed serial channel failed the loop back test. The valid bit reset pulse was extended to 30.9 nsec for FOXIE-07 to remove the timing issue in the high speed asynchronous serial channel. Once the valid bit reset pulse time was extended, all the asynchronous serial channels passed the loop back test

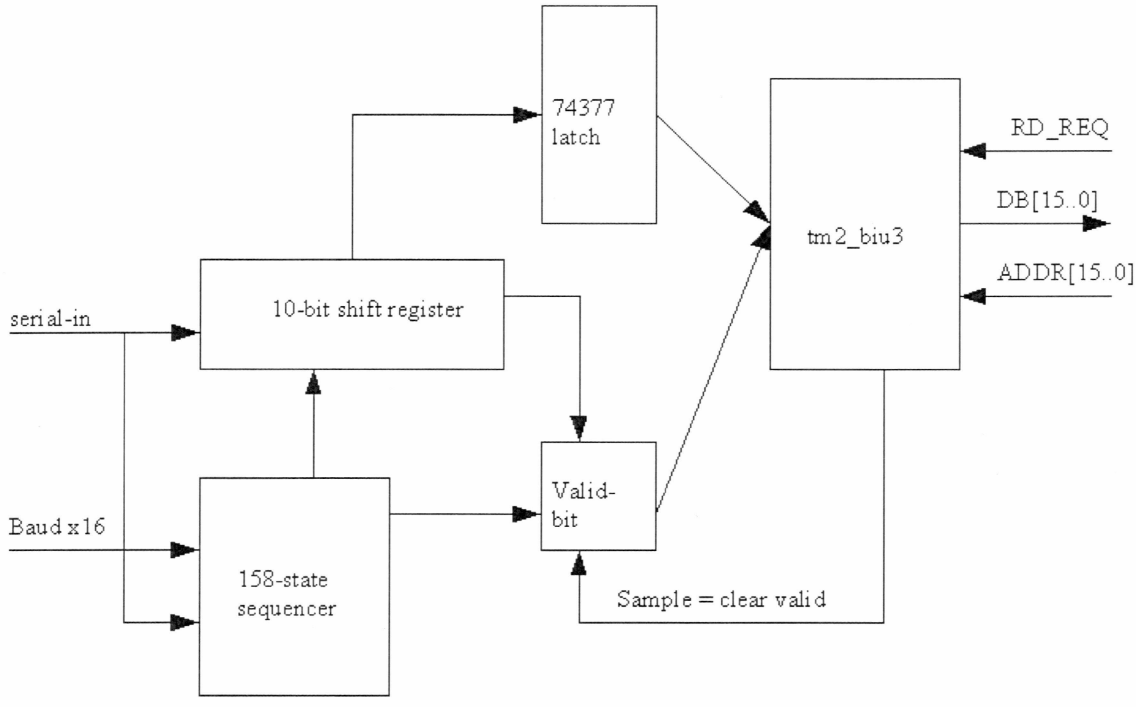


Figure 3-20 Block Diagram of Asynchronous Serial Controller

Testing of all the channels were performed as per the testing procedure provided in Chapter 5. All the channels passed the test without any crosstalk or timing issues in them.

3.5. Enhancements in MSP430 Coding

The MSP430F449 microcontroller interfaces with an AT25256A Atmel Serial EEPROM using the Serial Peripheral Interface (SPI) protocol. SPI is a synchronous serial data protocol used for communicating with one or more peripheral devices. With an SPI connection there is always one master device, generally the microcontroller, which controls the other peripheral devices. Three or four signals are used for data exchange [5] –

- SIMO – Slave in, master out.
    - Master mode - SIMO is the data output line.
    - Slave mode – SIMO is the data input line.
- SOMI – Slave out, master in.
    - Master mode – SOMI is the data input line.
    - Slave mode – SOMI is the data output line.
- UCLK – SPI clock.
    - Master mode – UCLK is an output.
    - Slave mode – UCLK is an input.
- STE – Slave transmit enable. Not used in 3-pin mode, in 4-pin mode used to allow multiple master on a single bus.

The firmware written for FOXIE-03 to read and write data from the EEPROM was bit-wise without using the SPI protocol, thus making the code lengthy. The new code uses 3-pin SPI mode for communicating and an extra pin for toggling the chip select pin of the EEPROM when data is read or written from the EEPROM. The clock required for synchronizing both the devices is provided by the master – microcontroller. Data transfer is initiated when the data is moved to the transmit buffer UxTXBUF. As soon as the TX shift register is empty it loads the data from UxTXBUF and transfers the data to the slave through the SIMO pin. Data from the slave is moved into the SOMI pin, which is moved to the receive shift register on the opposite clock edge. The received data is moved from the RX shift register to the receive data buffer UxRXBUF, and the receive interrupt flag URXIFGx is set indicating the completion of the operation.

The spi_transfer function shown below loads the output data into the transmit buffer, thus starting the SPI transmission. It then returns any data that has been shifted into the receive buffer by the EEPROM.

```
char spi_transfer (char data) {
```

```
while ((IFG2 & UTXIFG1) == 0);
TXBUF1 = data;
While ((IFG2 & URXIFG1) == 0);
return (RXBUF1);
}
```

The EEread function shown below reads data from the EEPROM. First the EEPROM is selected by the Port 4.2 of the MSP430. It is followed by the read instruction for the EEPROM, followed by the 16-bit address, Most Significant Bit first. These are followed by the transmission of a dummy byte to the EEPROM for the purpose of shifting the data out. Finally, the EEPROM is deselected using Port 4.2.

```
char EEread ( char ADDRH, char ADDRL ){
 P4OUT &= ~ (BIT2);            // assert CS
 spi_transfer (READ);          // Read Instruction
 spi_transfer (EEaddrH);       // Higher Address with the MSB first
 spi_transfer (EEaddrL);       // Lower Address
 data1 = spi_transfer (0xff);  // Dummy bits
 P4OUT |= BIT2;
 return (data1) ;}
```

3.6. Increase in Asynchronous Serial Baud Rate

The baud rates for the asynchronous serial channel were increased from 115.2 kbps to 460.8 kbps for FOXIE-07 to take care of the higher serial baud rate requirements for future missions. The increase in baud rate was achieved by the use of 36.38 MHz external clock and the internal PLL of the Cyclone FPGA to generate a 73.72 MHz clock. Standard serial baud rates from 1200 bps to 460.8 kbps were produced by taking the least common multiple of the all the required baud rates followed by prime-factor division of the 73.72 MHz clock. The 73.72 MHz clock was required as the

asynchronous serial channels are sampled 1.1 times the required baud rate for the channel. It was confirmed that the serial clocks don't show an error of more than 0.5% from the required baud rate clock. The 18.432 MHz clock required to generate the entire serial baud rate clock for FOXIE-03 was replaced by 36.86 MHz clock to achieve the higher baud rate for FOXIE-07.

3.7. Configuration Tool for the Data Matrix

The FOXIE-07 encoder follows the data matrix for FOXIE-03 which is provided in Appendix-A. The channels are arranged in the data matrix to maintain even symmetry between the different sampling rates. This section shows the calculation of the sampling rate for the data matrix and describes the tool that was designed to populate the matrix.

3.7.1. Sampling Rate Calculations

The equation used for calculating the data rate for fixed frame format is –

$$DR = WL * SFL * MF * FR \qquad \text{Equation [1]}$$

where DR is the bit rate, WL is the number of bits per word, SFL is the number of words per minor frame, MF is the number of minor frames per frame and FR is the frame rate. A given data rate will lead to a given frame rate.

For SRP5,

- DR = 800 kbps
- WL = 16
- Data matrix = 32 minor frames X 32 words (fixed)
- From data matrix, SFL = 32 and MF = 32
- Using Equation 1, Frame Rate = 48.82 frames per second (fps)

- Minor frame rate: 1562.24 mfps (minor frames per second)

A channel occurring once in the frame will have a sample rate equal to the Frame rate. For SRP5, the minimum sample rate required is 100 samples per second (sps) which can be achieved if a channel appears twice within the frame, since the frame rate for SRP5 data matrix is 48.83 fps. For example, sampling rate for CH0 occurring twice in the data matrix is (48.82 X 2) 97.56 sps. Table 3-1 shows the requested sample rate, the actual sample rate and the number of times the channels are sampled in a major frame. Special care has to be taken for calculating the sampling rate of serial data, which is loaded as parallel data into a register. In this case a 9^{th} bit is used to indicate the reception of a "valid" data. The calculations for a 115.2 kbps data source S0 in data matrix was carried-on as –

> 115.2 kbps yields a maximum word rate of 11,520 words/sec assuming 8N1 data in which one start bit and one stop bit is added for each 8 bits of data. One needs to sample at 110% of the word rate to ensure that none are missed. Thus we need to sample at 12.672 ksps for a 115.2 kbps serial channel. The required sample rate can be achieved if the data is sample at 32 X 8 X 48.82 times. Thus a serial channel with a bit rate of 115.2 kbps (or 12.7 ksps) has to appear 32 X 8 times in the data matrix.

From table 3-1 total numbers of words used by the channels in the data matrix are 956 out of 1064 words available. 68 words are used for overhead in the data matrix for synchronization of the telemetry data stream. SRP5 uses only 42 analog channels of the total 64 analog channels. Similarly, 4 asynchronous serial channels are used out of the 8 available serial channels. These unused channels can be used for future mission with an increase in the data rate to accommodate video or other types of high speed data.

3.7.2. Configuration Tool

A spreadsheet using Microsoft Excel was created to input a data matrix and convert it to

Table 3-1 Sampling rate for different channels

Channels Description	Sampling Rate	Number of Channels	Actual Sampling Rate	Number of occurrences in data matrix	Number of Words
Analog Channel	100 sps	42	97.65 sps	2	84
Analog Channel	1.0 ksps	8	1.52 ksps	32	256
Analog Channel	2.0 ksps	3	3.12 ksps	64	192
Serial Channel	115.2 kbps	1	12.7 ksps	256	256
Serial Channel	19.2 kbps	2	3.12 ksps	64	128
Serial Channel	19.2 kbps	1	1.52	32	32
Parallel Channel	100 sps	4	97.65 sps	2	8

[Note: Many channels are sampled higher than requested]

the format required by the FOXIE-07 EEPROM. The data matrix can be populated according to mission requirements. Special function registers, as given in Appendix-D, are provided in the spreadsheet to modify the dimensions of the data matrix and the data rate required for the mission. Hexadecimal addresses were assigned for each of the channels in the data matrix as well as for the special function registers, given in Appendix-D. The macro program running within the spreadsheet can translate the hexadecimal channel address into the Intel Hex format for burning into the EEPROM on the FOXIE-07 encoder. Intel Hex is a format for conveying binary information for applications like programming microcontroller, EEPROM and other kinds of chips. It is divided into 6 parts –

1. Start code - a colon ':'.
2. Byte count - two hex digits equal to the number of bytes (n) in the data field.
3. Start Address - four Hex digits equal to the starting address of the data in memory.
4. Record type - two hex digits defining the type of the data field.

00 - always data

01 - End of file record

02 - Extended segment address record

03 - Start segment address record

04 - Extended linear address record

05 - Start linear address record.

5. Data - a sequence of n bytes of the data themselves.
6. Checksum - two hex digits of the least significant byte of the two's complement sum of the values of all fields except fields 1 and 6.

The EEPROM chosen for the FOXIE encoder is Atmel's AT25256A. It is a 256-kbit serial EEPROM with an SPI interface. The AT25256A is capable of storing 8-bit data into a 16-bit address. Thus the macro stores 8-bit data in 16-bit addressing mode using the big-endian format; e.g., the MSB of the first data was stored in 0x00H and the LSB in 0x01H and it continues for the next data. A graphical user interface named TACOSMATRIX was developed using National Instruments LabWindows CVI8.1 to simply configuring a new data matrix. Figure 3-21 shows the flow chart of the macro within the excel spreadsheet and Figure 3-22 shows the TACOSMATRIX user interface software. The software can be operated by running the TACOSMATRIX.exe file. The user needs to perform these steps for setting up the data matrix into the EEPROM through the TACOSMATRIX software.

- The LaunchExcel button is used to open Microsoft Excel spreadsheet.
- The tm.xls spreadsheet can be opened using the OpenFile button.
- The SaveFile can be used to save if any modifications are made in the data matrix.
- The Run button is used to run the macro inside the spreadsheet, the IntelHex file is generated in the default directory (e.g., My Documents on the computer).
- The CloseFile button is used to close the excel file.

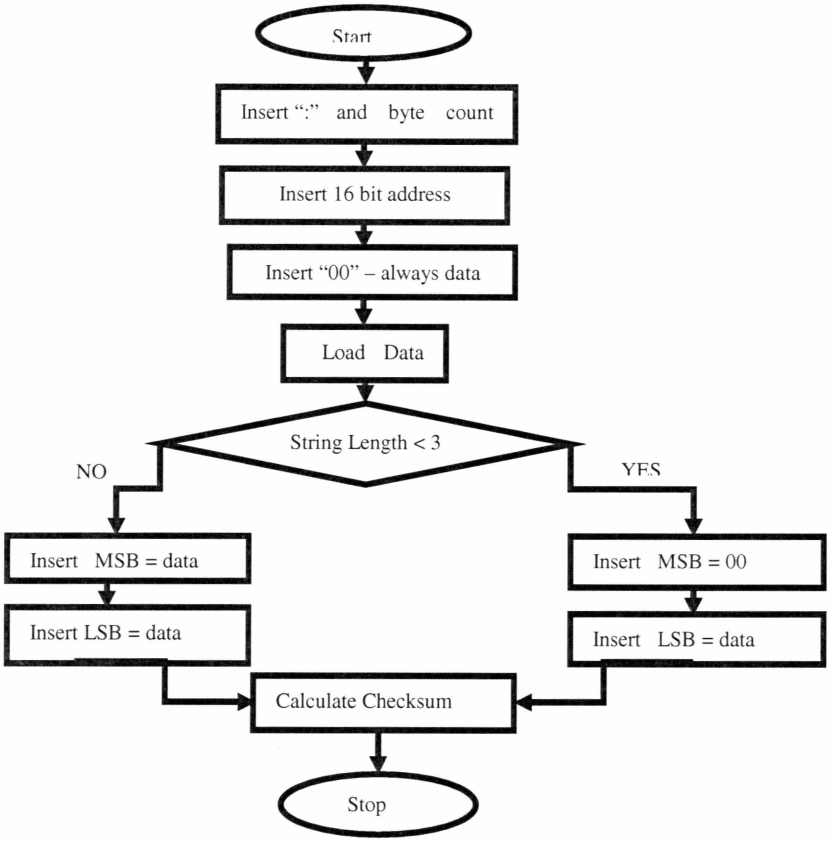


Figure 3-21 Flow Chart for the Macro

- The Quit button is used to close the application.
- Print button can be used to print the data matrix.
- An EEPROM programmer such as EE Tools TOP-MAX programmer can be used to burn the Intel Hex file into the EEPROM.
- Once the EEPROM is loaded with the data matrix it is inserted into the socket provided in the core board of FOXIE.

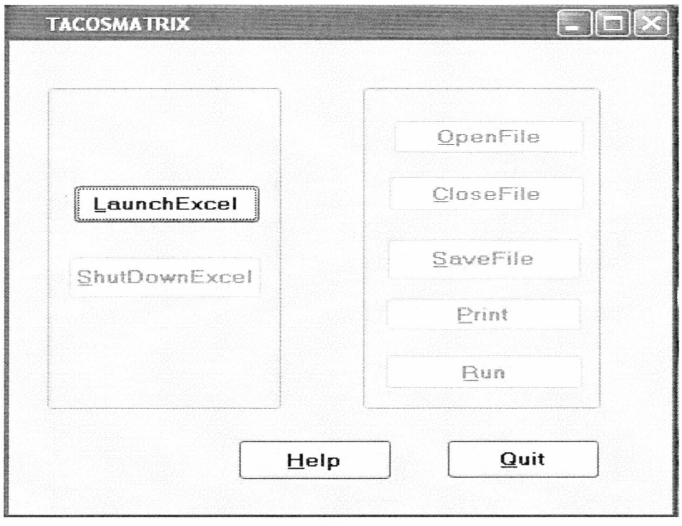


Figure 3-22 TACOSMATRIX Software

3.8. Ground Support Data Feed

The ASRP ground support requested to have a display of all the channels and there outputs at the ground support for monitoring the channels before launch. Consequently, it is decided to stream the telemetry data link from the FOXIE-07 to the ground support through the "Umbilical Interface" on the rocket payload. The ground station will have a decoder board for decoding the data. The only viable approach is to use the fiber-optics transmitter provided in the core board as a communication link with the rocket "Umbilical Interface". The fiber-optics transmitter chosen for this purpose is IF-E96 from Industrial Fiber-Optics. The IF-E96 uses a red LED having a peak wavelength of 660 nm. It has a rise time and a fall time of 0.1 μsec. The fast rise and fall times of the IF-E96 permits data rate up to 5 Mbps, making it suitable to transmit the high data rate for SRP5. The IF-E96 produces an inverted output so the "Umbilical Interface" should have an inverter followed with IF-D97 optical fiber receiver for proper reception of the high speed data.

CHAPTER - 4

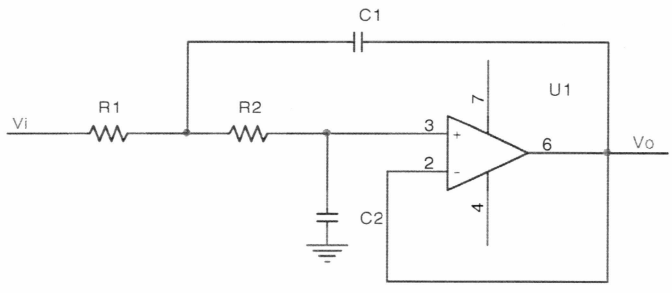
Pre-Modulation Filter

4.1. Introduction

The modulation technique utilized for the SRP5 mission is Pulse Code Modulation (PCM) / Frequency Modulation (FM). The NRZ-L PCM output from the FOXIE encoder is used to frequency modulate the carrier. The NRZ-L signal from the FOXIE encoder resembles a square waveform with steep rise and fall times. The steep transition times of the square wave give rise to a broad spectrum with unwanted harmonics. The unwanted harmonics of the square wave can be removed by using a low-pass filter. A low-pass pre-modulation filter is used between the FOXIE encoder and the frequency modulator to eliminate the undesired harmonics, thereby limiting the frequency bandwidth of the transmitted signal. A good choice for a pre-modulation filter is a multi-pole filter with bandwidth equal to 0.7 times the bit rate [2].

4.2. Design and Implementation of Pre-modulation Filter

A second-order low-pass Butterworth Sallen-Key filter was implemented as the pre-modulation filter for the SRP5 telemetry system. Figure 4-1 shows a second-order Sallen-Key low-pass filter.



$R_1=R_2=1k\Omega$ $C_1=C_2=120$ pF

Figure 4-1 Second order Sallen-Key Low Pass Filter

The operations of a Sallen-Key filter can be described as follows:

- At low frequencies, where C1 and C2 appear as open circuits, the signal is simply buffered to the output.
- At high frequencies, where C1 and C2 appear as short circuits, the signal is shunted to ground at the amplifier's input thereby attenuating the signal at the output.
- At cut-off frequency, where the impedance of C1 and C2 is of the same order as R1 and R2, positive feedback through C2 provides Q enhancement of the signal.

The transfer function of the Sallen-Key filter is given as –

$$T(s) = \left(\frac{1}{C1C2R1R2s^2 + C2(R1+R2)s + 1} \right). \qquad \text{Equation [2]}$$

The Q-factor and cut-off frequency is given by equations 3 and 4 –

$$Q = \left(\frac{\sqrt{R_1 R_2 C_1 C_2}}{C_2(R_1 + R_2)} \right) \qquad \text{Equation [3]}$$

$$F = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}. \qquad \text{Equation [4]}$$

The op-amp LM6647 was chosen as the amplifier for the filter. It is a rail-to-rail input and output voltage feedback amplifier, offering high speed and low voltage operation. It is generally used for active filter design. The pre-modulation filter has a cut-off frequency of 1.3 MHz. Frequency response of the pre-modulation filter is shown in Figure 4-2. Figure 4-3 shows the NRZ-L baseband signal from FOXIE encoder and Figure 4-4 shows the output of the pre-modulation filter.

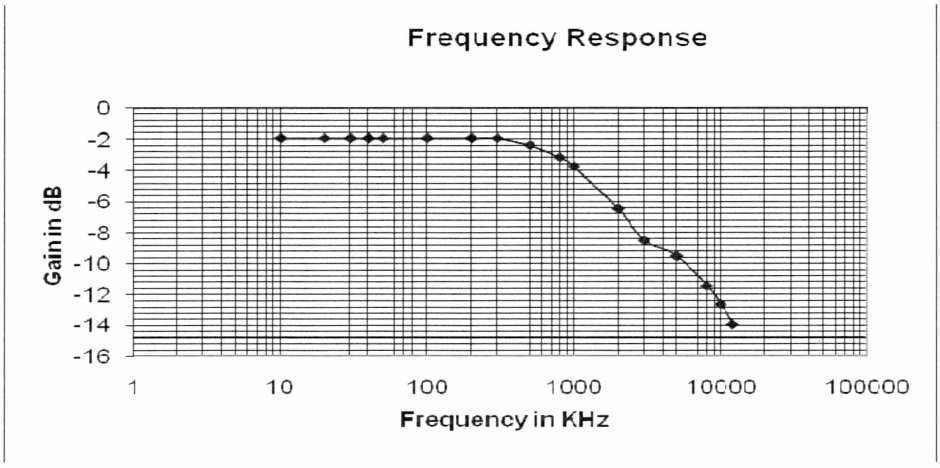


Figure 4-2 Frequency Response of the Pre-modulation Filter

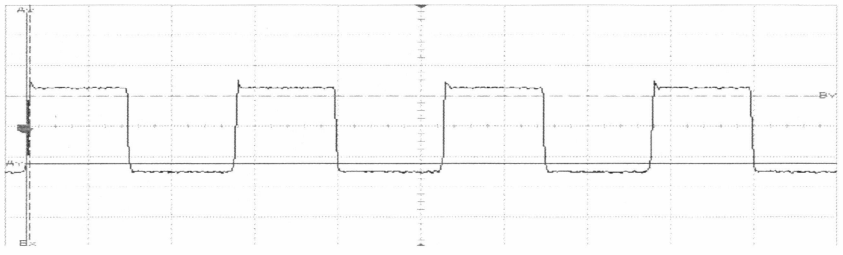


Figure 4-3 NRZ-L Baseband signal from the FOXIE encoder

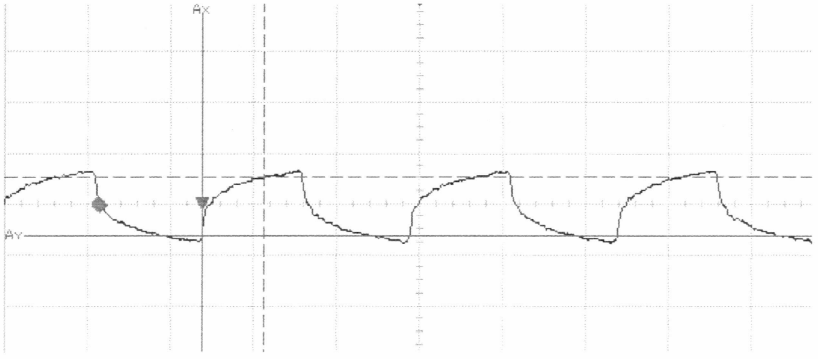


Figure 4-4 Pre-modulation Filter Output

Once the design prototype was tested and verified, the next step was to layout a PCB. The OrCAD Layout software was used to layout a small board of 2365 by 2364 mils for the pre-modulation filter. The components were all SMD (Surface Mount Devices) type, with a DB-9 connector for the input and an SMA connector for the output. The signal traces are set to a width of 8 mils and a trace–to–trace spacing of 12 mils. The power and ground trace widths were all kept at 12 mils. Figure 4-5 shows a routed board before applying ground planes and Figure 4-6 shows the fabricated pre-modulation filter board.

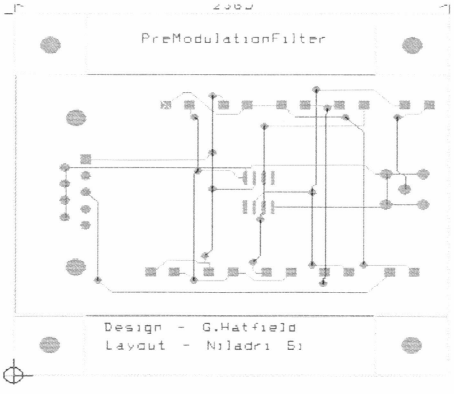


Figure 4-5 Pre-modulation Filter Board Layout

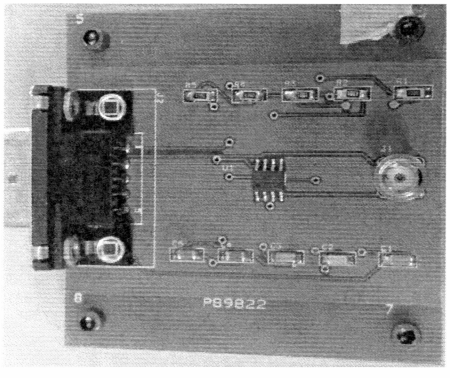


Figure 4-6 Fabricated Pre-modulation Filter

4.3. Pre-Modulation Filter Testing

To verify the performance of the pre-modulation filter, the following tests were conducted. A test setup was made as shown in Figure 4-7 to observe the spectrum of the frequency modulated signal without the pre-modulation filter implemented. Agilent E4433B Signal Generator was used to generate a carrier frequency of 2.2 GHz with frequency modulation. The frequency deviation was set as 560 kHz and the Spectrum Analyzer was used for observing the spectrum. The NRZ-L signal from FOXIE is used as the modulating signal. A similar test setup was made with the introduction of the pre-modulation filter as shown in Figure 4-8. The 3.3 Vp-p NRZ-L signal from FOXIE is attenuated to 1.6 Vp-p signal by the pre-modulation filter. This 1.6 Vp-p signal was applied as an input to the signal generator. But no gain adjustment in the signal generator was made during the test to compensate for this attenuation in the modulating signal.

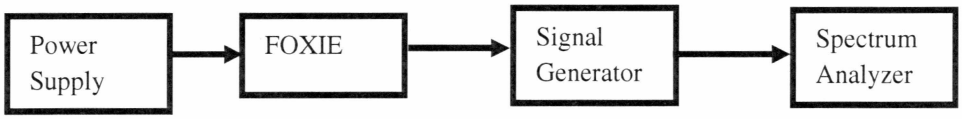


Figure 4-7 Test setup without Pre-modulation Filter

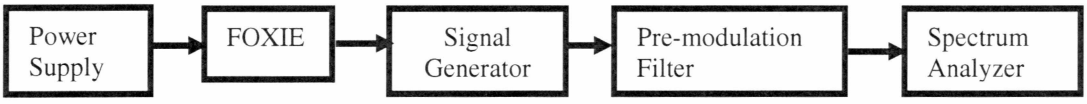


Figure 4-8 Test setup with the Pre-modulation Filter

Figure 4-9 and Figure 4-10 shows the frequency spectrum without and with the introduction of the pre-modulation filter. From the figures it can be concluded that the

pre-modulation filter was successful in removing spurious harmonics from the telemetry stream. But it was also observed that the pre-modulation filter was filtering the first side-band thereby losing the information contained in the telemetry stream.

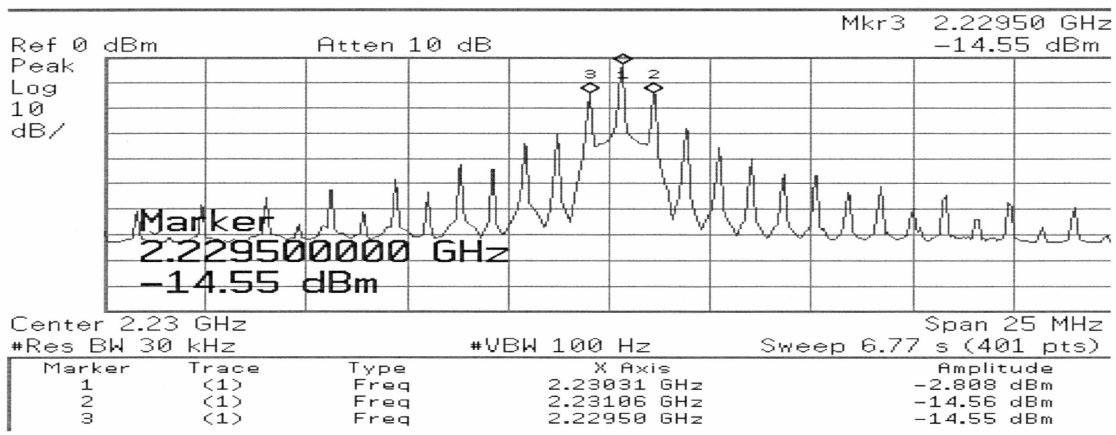


Figure 4-9 Spectrum of the Telemetry Stream without Pre-modulation Filter

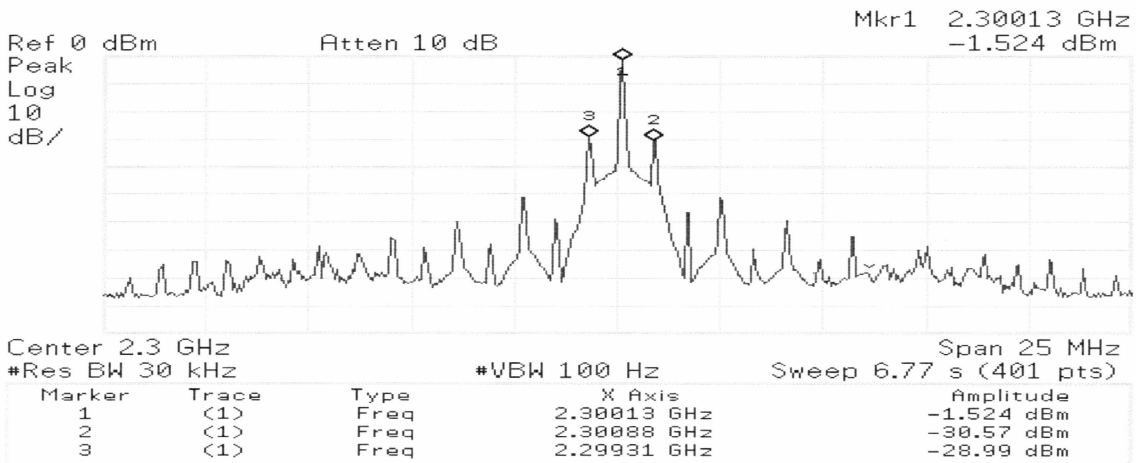


Figure 4-10 Spectrum of the telemetry stream with Pre-modulation Filter

CHAPTER - 5

Telemetry System Testing

5.1. Introduction

The FOXIE-07, encoder was configured for the SRP5 mission and then evaluated through a series of tests before being qualified as flight hardware. Figure 5-1 shows the life cycle of FOXIE-07 from building the hardware followed by the acceptance and environmental test. All the tests that were being specified for FOXIE-03 were taken as a guideline for the tests of FOXIE-07[1].

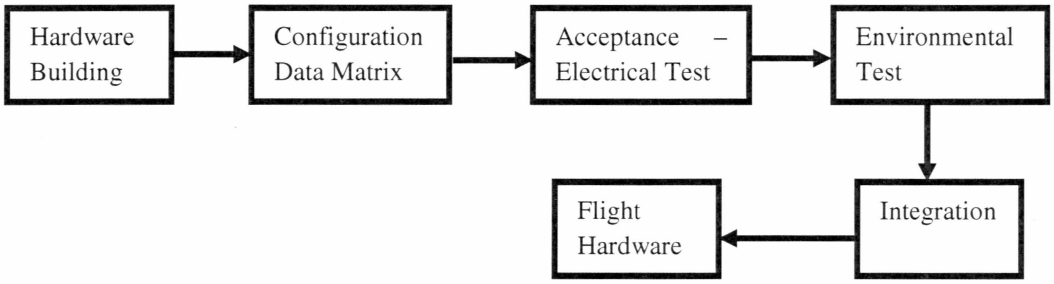


Figure 5-1 Life Cycle for FOXIE Hardware Qualification

5.2. Electrical Acceptance Test

A successful completion of all these tests certifies the FOXIE-07 electrically for integration into the rocket payload.

5.2.1. Electrical Burn-in Tests

The purpose of this test is to ensure that the Device under Test (DUT) will not fail after longer periods of operation. The test procedure is –

- Configure the DUT (FOXIE-07) with the desired data matrix and special function registers.
- Power the DUT to the specified voltage levels (+12 V).
- Connect the decoder device of Stephen Bruss to monitor the output of the encoder.
- Leave power on for 24 hours.
- Observe the equipment every 1 hour to verify operation.

Results: PacketErrorRate after 24 hour – 2.54×10^{-6}

5.2.2. Power Extremity Tests

The purpose of this test is to verify if the power supply range is within its limit. The test is performed with the following steps –

- Configure the DUT (FOXIE-07) with the desired data matrix and special function registers.
- Power the DUT to the specified voltage levels (+12 V).
- Connect the decoder device of Stephen Bruss to monitor the output of the encoder.
- Record the current drawn by the FOXIE–07.
- Repeat for +15 V and +9 V.

Results: Current drawn: 187 mA at +15 V
225 mA at +12 V

270 mA at +9 V

5.2.3. Analog Channel Tests

The analog channel tests are conducted for a complete verification of all analog channels. The procedure for the analog test is as follows –

- Configure the DUT (FOXIE-07) with the desired data matrix and special function registers.
- Power the DUT to the specified voltage levels (+12 V).
- Connect the decoder device of Stephen Bruss to monitor the output of the encoder.
- Connect the analog inputs to a power supply capable of delivering ±10 V.
- Display all the channels with the decoder device.
- Apply 0 V, +/- 2.5 V, +/- 5 V, +/- 7.5 V and +/- 10 V to the analog inputs.
- Apply a 10 Vp-p, 1 Hz sine wave to the analog inputs.
- Record all the observed results in the test sheet.

Results – All the analog channels passed the test without any crosstalk. It is recommended to increase the sample buffer (more than 10,000) in Stephen Bruss display software during real time plotting of the high speed analog channels.

5.2.4. Parallel Channel Tests

The parallel channel tests are conducted for a complete verification of all parallel channels. The procedure for the parallel test is as follows –

- Configure the DUT (FOXIE-07) with the desired data matrix and special function registers. Power the DUT to the specified voltage levels (+12 V). Connect the decoder device of Stephen Bruss to monitor the output of the encoder.

- Apply inputs by using a DIP switch and a power supply (+5 V), toggle the DIP switch to verify each bit.
- Reduce the power supply until the bits are oscillating, this is the logical transition voltage and should be near to 1.85 V.
- Successful completion of the test verifies that the parallel channels are working.

Results: The parallel channels passed the test without any crosstalk.

5.2.5. Asynchronous Serial Channel Tests

The loop back test is used to verify the asynchronous serial channels. The test set-up is as shown in Figure 5-2.
The procedure for the asynchronous serial test is as follows –

- Configure the DUT (FOXIE-07) with the desired data matrix and special function registers.
- Power the DUT to the specified voltage levels (+12 V).
- Set up the test equipment as shown in Figure 5-2.
- On Computer – 2 run WinSSD software and Stephen Bruss Decoder Display Software on Computer -1.
- Setup the decoder *.ini file to output the desired serial port data.
- Setup WinSSD to communicate on the desired baud rate.
- Run WinSSD loop back tests with timeout multipliers set to 1000 in WinSSD software.
- Successful completion of the test verifies that the asynchronous serial channels are working.

Results: All the asynchronous serial channels passed the loop back test.

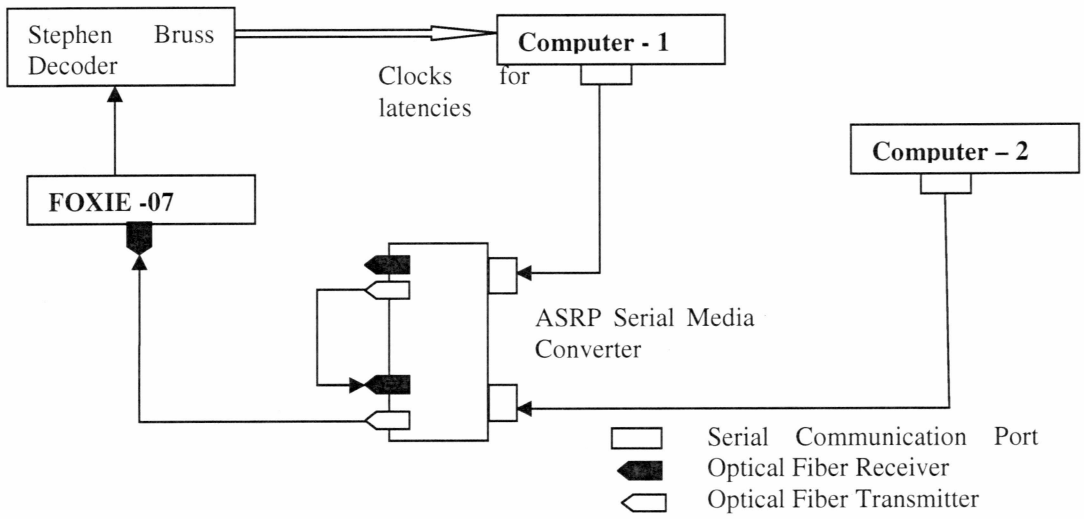


Figure 5-2 Loop back test set-up

5.3. Environmental Acceptance Test

Once the FOXIE-07 succeeds the Electrical Acceptance Tests, it has to go through the Environmental Acceptance Tests. The environmental tests authenticate the FOXIE-07's performance in less ideal conditions. It can be divided into two basic types – thermal and vibration tests. Environmental test were not conducted on the prototype core board. The environmental test will be completed after the new 8-layer core board is assembled and tested.

5.3.1. Thermal Test

The thermal tests are conducted in the environmental chamber possessed by the Mechanical Department of the UAF. The procedure for the test is as follows –

- Configure the DUT (FOXIE-07) with the desired data matrix and special function registers.
- Power the DUT to the specified voltage levels (+12 V). Connect the decoder device of Stephen Bruss to monitor the output of the encoder.

- Insert the FOXIE-07 into the thermal chamber; vary the temperature from -4 °F to 104 °F, monitor the performance of the FOXIE-07 by observing the PacketErrorRate in Stephen Bruss's Software. Repeat the steps for 2 cycles.
- Finally let the instrument standing at -4 °F from 45 minutes and then power it to observe its behavior.
- Successful completion of the test verifies that the FOXIE-07 working under different thermal conditions.

5.3.2. Vibration Test

The vibration tests are conducted with the vibration table possessed by the Mechanical Department of the UAF. The procedure for the test is as follows –

- Configure the DUT (FOXIE-07) with the desired data matrix and special function registers. Power the DUT to the specified voltage levels (+12 V).
- Connect the decoder device of Stephen Bruss to monitor the output of the encoder.
- Place the FOXIE-07 on the vibration table vibrate the FOXIE-07 as per vibration requirements for the mission.
- Repeat the steps for 2 cycles.
- Successful completion of the test verifies that the FOXIE-07 working under vibration.

5.4. Test Results

Extensive testing of all the serial, analog and parallel channels was done as per the testing procedure. The FOXIE-07 successfully passed all the Electrical Tests. Appendix-C provides a summary of the test results.

CHAPTER - 6

Conclusions and Future Work

6.1. Conclusions

The FOXIE-07 is fully tested using the Ground Support Software of Stephen Bruss. From the results it is verified that all the crosstalk in the channels are removed successfully. The FOXIE-07 is significantly documented and members of ASRP are trained in its operation and testing. The FOXIE-07 meets the entire goal set for the thesis:

- Removal of crosstalk in the analog channels.
- Removal of timing issue in the asynchronous serial channel.
- Removal of thermal issue from the analog board.
- Providing a flight-ready encoder for SRP5 mission.
- Implementation of the pre-modulation filter.

Figure 6-1 shows the FOXIE-07 fully assembled and ready for integration with the SRP5 payload.

6.2. Future Work

FOXIE-07 is essentially an upgrade to FOXIE-03 in terms of eradicating channel crosstalk and also eliminating some of the software issues responsible for non functionality of some channels. As a result, the upgrades recommended for future revisions of FOXIE-03 [1] were not implemented. Consequently, future revisions of the FOXIE can be upgraded by the following ways –

- An Ethernet–to–Serial gateway for networking within the rocket can be provided.

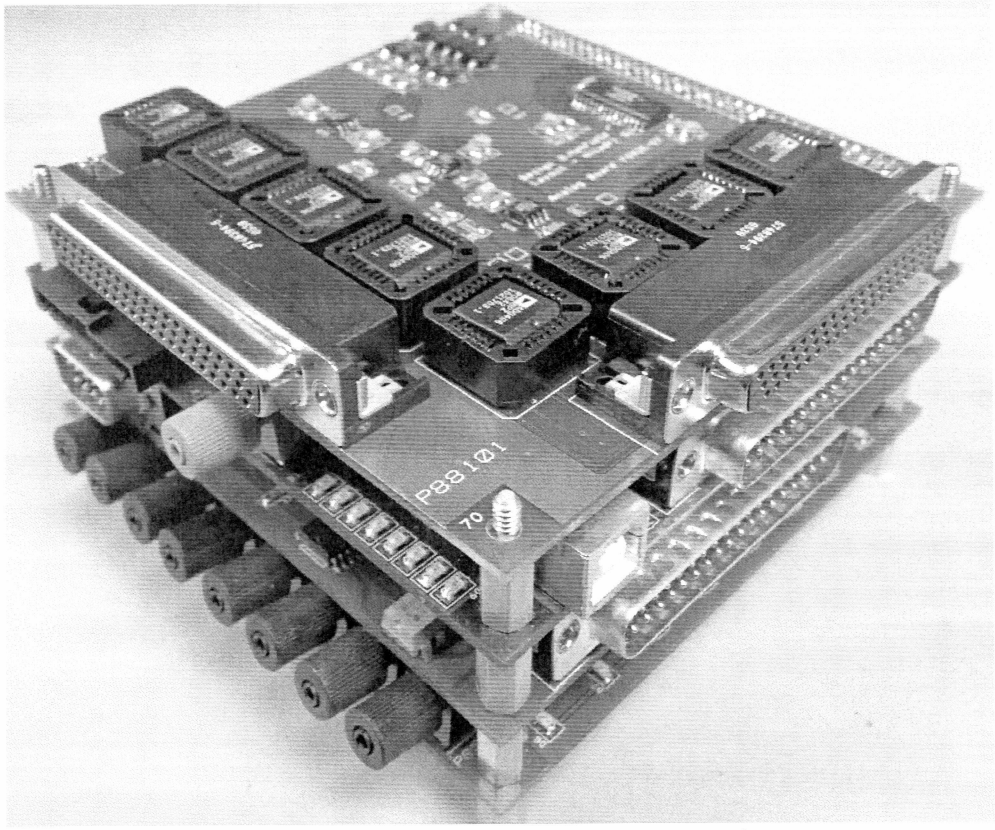


Figure 6-1 FOXIE-07 Fully Integrated

- A real-time data link can be provided for instruments on the rocket allowing them to pre-process data and then reinsert it into the telemetry stream. A real time flight computer could share FOXIE's digitized data over a high speed serial link thereby reducing the complexity of flight computer design and also reduce the number of components and cable needed for a payload.

References

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Appendix-A

Channel Assignments

A-1 Telemetry Channel Assignments

Analog Channels

Table A-1 Analog Channel Descriptions

Channel Abbreviation	Description	Required Sampling Rate	Acquired Sampling Rate
ACHO	Power System Current Monitor (+15 V)	100 sps	97.5 sps
ACH1	Power System Current Monitor (+12 V)	100 sps	97.5 sps
ACH2	Power System Current Monitor (+5 V)	100 sps	97.5 sps
ACH3	Power System Current Monitor (+3.3 V)	100 sps	97.5 sps
ACH4	Power System Current Monitor (-15 V)	100 sps	97.5 sps
ACH5	Power System Voltage Monitor (+15 V)	100 sps	97.5 sps
ACH6	Power System Voltage Monitor (+12 V)	100 sps	97.5 sps
ACH7	Power System Voltage Monitor (+5 V)	100 sps	97.5 sps
ACH8	Power System Voltage Monitor (+3.3 V)	100 sps	97.5 sps
ACH9	Power System Voltage Monitor (-15 V)	100 sps	97.5 sps
ACH10	Ambient Temperature 1 (Power System)	100 sps	97.5 sps

Table A-1 continued

ACH11	Ambient Temperature 2 (Power System)	100 sps	97.5 sps
ACH12	Ambient Temperature 3 (Flight Instruments)	100 sps	97.5 sps
ACH13	Battery Temperature	100 sps	97.5 sps
ACH14	Pressure Sensor 1	100 sps	97.5 sps
ACH15	Pressure Sensor 2	100 sps	97.5 sps
ACH16	TPU Radio CH1 waveform	2.0 ksps	3.12 ksps
ACH17	TPU Radio CH2 waveform	2.0 ksps	3.12 ksps
ACH18	TPU Radio CH3 waveform	2.0 ksps	3.12 ksps
ACH20	Accelerometer " X"	1.0 ksps	1.56 ksps
ACH21	Accelerometer "Y"	1.0 ksps	1.56 ksps
ACH22	Accelerometer "Z"	1.0 ksps	1.56 ksps
ACH23	Accelerometer "R"	1.0 ksps	1.56 ksps
ACH24	Accelerometer "T"	1.0 ksps	1.56 ksps
ACH25	TM Magnetometer "X"	100 sps	97.5 sps
ACH26	TM Magnetometer "Y"	100 sps	97.5 sps
ACH27	TM Magnetometer "Z"	100 sps	97.5 sps
ACH31	Thermocouple CH0	100 sps	97.5 sps
ACH32	Thermocouple CH1	100 sps	97.5 sps
ACH33	Thermocouple CH2	100 sps	97.5 sps
ACH34	Thermocouple CH3	100 sps	97.5 sps
ACH35	Thermocouple CH4	100 sps	97.5 sps
ACH36	Thermocouple CH5	100 sps	97.5 sps
ACH37	Thermocouple CH6	100 sps	97.5 sps
ACH38	Thermocouple CH7	100 sps	97.5 sps
ACH39	Thermocouple CH8	100 sps	97.5 sps
ACH40	Thermocouple CH9	100 sps	97.5 sps
ACH41	Thermocouple CH10	100 sps	97.5 sps
ACH42	Thermocouple CH11	100 sps	97.5 sps

Table A-1 continued

ACH43	0 V Reference	N/A	
ACH49	Tokai UV Sensor CH0 (UV)	100 sps	97.5 sps
ACH50	Tokai UV Sensor CH1 (VIS)	100 sps	97.5 sps
ACH51	TPU Radio Temperature Sensor	100 sps	97.5 sps
ACH52	Tokai Magnetometer "X"	1.0 ksps	1.56 ksps
ACH53	Tokai Magnetometer "Y"	1.0 ksps	1.56 ksps
ACH54	Tokai Magnetometer "Z"	1.0 ksps	1.56 ksps
ACH55	TPU Radio CH1 "HIGH"	100 sps	97.5 sps
ACH56	TPU Radio CH2 "HIGH"	100 sps	97.5 sps
ACH57	TPU Radio CH3 "HIGH"	100 sps	97.5 sps
ACH58	TPU Radio CH1 "LOW"	100 sps	97.5 sps
ACH59	TPU Radio CH2 "LOW"	100 sps	97.5 sps
ACH60	TPU Radio CH3 "LOW"	100 sps	97.5 sps

Serial Channels

Table A-2 Serial Channel Descriptions

Channel Abbreviation	**Description**	**Requested Baud Rate**	**Acquired Sample Rate**
S0	Plasma Probe	115.2 k	12.7 ksps
S1	IMU Serial Data	19.2 k	2.2 ksps
S2	SMU Serial Data	19.2 k	2.2 ksps
S3	UAF GPS	9600	2.2 ksps
S4	Not Used		
S5	Not Used		
S6	Not Used		
S7	Not Used		

Parallel Channels (8 bits each)

Table A-3 Parallel Channel Descriptions

Channel Abbreviation	Description	Requested Sample Rate	Acquired Sample Rate
P0	Unused	100 sps	97.5 sps
P1	TC Alarms (Main)	100 sps	97.5 sps
P2	TC Alarms (Auxiliary)	100 sps	97.5 sps
P3	TPU Sun Sensor	100 sps	97.5 sps

Other Channels

SFID: Sub-frame ID (value = 0000H to 001FH); URC = 0x001F, Pos 1 (for TDP)

SW: Sync-word, EB90 (Hex), subject to change. Mask = 0xFFFF0000 (for GDP)

TSA: Time Stamp A (16 MSB's of Time Stamp Counter.)

TSB: Time Stamp B (8 LSB's of Time Stamp Counter + checksum. Updates at 20.48 milliseconds)

Table A-4 TSA

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS 23	TS 22	TS 21	TS 20	TS 19	TS 18	TS 17	TS 16	TS 15	TS 14	TS 13	TS 12	TS 11	TS 10	TS 9	TS 8

Table A-5 TSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS7	TS6	TS5	TS4	TS3	TS2	TS1	TS0	CK7	CK6	CK5	CK4	CK3	CK2	CK1	CK0

CK7...0 = TS23...16 + TS15...8 + TS7...0, no carry's

A-2 Data Matrix

	0	1	2	3	4	24	25	26	27	28	29	30	31
0	SW	SFID	S0	ACH16	ACH17	S2	ACH24	S0	ACH49	S3	ACH7	S0	ACH37
1	SW	SFID	S0	ACH16	ACH17	S2	ACH24	S0	ACH50	S3	ACH8	S0	ACH38
2	SW	SFID	S0	ACH16	ACH17	S2	ACH24	S0	ACH51	S3	ACH9	S0	ACH39
3	SW	SFID	S0	ACH16	ACH17	S2	ACH24	S0	ACH55	S3	ACH14	S0	ACH40
4	SW	SFID	S0	ACH16	ACH17	S2	ACH24	S0	ACH56	S3	ACH15	S0	ACH41
5	SW	SFID	S0	ACH16	ACH17	S2	ACH24	S0	ACH57	S3	ACH13	S0	ACH42
6	SW	SFID	S0	ACH16	ACH17	S2	ACH24	S0	ACH58	S3	ACH43	S0	P0
7	SW	SFID	S0	ACH16	ACH17	S2	ACH24	S0	ACH59	S3	ACH10	S0	P1
8	SW	SFID	S0	ACH16	ACH17	S2	ACH24	S0	ACH60	S3	ACH11	S0	P2
9	SW	SFID	S0	ACH16	ACH17	S2	ACH24	S0	ACH0	S3	ACH12	S0	P3
10	SW	SFID	S0	ACH16	ACH17	S2	ACH24	S0	ACH1	S3	ACH31	S0	ACH43
11	SW	SFID	S0	ACH16	ACH17	S2	ACH24	S0	ACH2	S3	ACH32	S0	ACH25
12	SW	SFID	S0	ACH16	ACH17	S2	ACH24	S0	ACH3	S3	ACH33	S0	ACH26
13	SW	SFID	S0	ACH16	ACH17	S2	ACH24	S0	ACH4	S3	ACH34	S0	ACH27
14	SW	SFID	S0	ACH16	ACH17	S2	ACH24	S0	ACH5	S3	ACH35	S0	TSA
15	SW	SFID	S0	ACH16	ACH17	S2	ACH24	S0	ACH6	S3	ACH36	S0	TSB
16	SW	SFID	S0	ACH16	ACH17	S2	ACH24	S0	ACH49	S3	ACH7	S0	ACH37
17	SW	SFID	S0	ACH16	ACH17	S2	ACH24	S0	ACH50	S3	ACH8	S0	ACH38
18	SW	SFID	S0	ACH16	ACH17	S2	ACH24	S0	ACH51	S3	ACH9	S0	ACH39
19	SW	SFID	S0	ACH16	ACH17	S2	ACH24	S0	ACH55	S3	ACH14	S0	ACH40
20	SW	SFID	S0	ACH16	ACH17	S2	ACH24	S0	ACH56	S3	ACH15	S0	ACH41
21	SW	SFID	S0	ACH16	ACH17	S2	ACH24	S0	ACH57	S3	ACH13	S0	ACH42
22	SW	SFID	S0	ACH16	ACH17	S2	ACH24	S0	ACH58	S3	ACH43	S0	P0
23	SW	SFID	S0	ACH16	ACH17	S2	ACH24	S0	ACH59	S3	ACH10	S0	P1
24	SW	SFID	S0	ACH16	ACH17	S2	ACH24	S0	ACH60	S3	ACH11	S0	P2
25	SW	SFID	S0	ACH16	ACH17	S2	ACH24	S0	ACH0	S3	ACH12	S0	P3
26	SW	SFID	S0	ACH16	ACH17	S2	ACH24	S0	ACH1	S3	ACH31	S0	ACH43
27	SW	SFID	S0	ACH16	ACH17	S2	ACH24	S0	ACH2	S3	ACH32	S0	ACH25
28	SW	SFID	S0	ACH16	ACH17	S2	ACH24	S0	ACH3	S3	ACH33	S0	ACH26
29	SW	SFID	S0	ACH16	ACH17	S2	ACH24	S0	ACH4	S3	ACH34	S0	ACH27
30	SW	SFID	S0	ACH16	ACH17	S2	ACH24	S0	ACH5	S3	ACH35	S0	TSA
31	SW	SFID	S0	ACH16	ACH17	S2	ACH24	S0	ACH6	S3	ACH36	S0	TSB

Appendix-B

Test Results of FOXIE-03

Table B-1 Test Results of FOXIE-03

Channels	Sampling Rate	Notes
Analog Channel 0	100 sps	Passed
Analog Channel 1	100 sps	Passed
Analog Channel 2	100 sps	Passed
Analog Channel 3	100 sps	Passed
Analog Channel 4	100 sps	Passed
Analog Channel 5	100 sps	Passed
Analog Channel 6	100 sps	Passed
Analog Channel 7	100 sps	Passed
Analog Channel 8	100 sps	Passed
Analog Channel 9	100 sps	Passed
Analog Channel 10	100 sps	Passed
Analog Channel 11	100 sps	Passed
Analog Channel 12	100 sps	Passed
Analog Channel 13	100 sps	Passed
Analog Channel 14	100 sps	Passed
Analog Channel 15	100 sps	Values changes from positive to negative very fast
Analog Channel 16	2 ksps	Same values are repeated in Analog Channel 17
Analog Channel 17	2 ksps	Values are shown in Analog Channel 18 instead of Analog Channel 17
Analog Channel 18	2 ksps	Channel Feed through with magnitude < 0.8 with random spikes

Table B-1 continued

Analog Channel 19		Not used
Analog Channel 20	1 ksps	Values are shown in Analog Channel 22 instead of Analog Channel 20
Analog Channel 21	1 ksps	Feed through on to Analog Channel 23 and Analog Channel 22 with 1/10 voltage
Analog Channel 22	1 ksps	Values are shown at Analog Channel 23 instead of Analog Channel 22
Analog Channel 23	1 ksps	Obtained values are never more than 0 volts
Analog Channel 24	1 ksps	Other Channels also shows values less than 1 volts
Analog Channel 25	100 sps	Passed
Analog Channel 26	100 sps	Passed
Analog Channel 27	100 sps	Passed
Analog Channel 28		Not used
Analog Channel 29		Not used
Analog Channel 30		Not used
Analog Channel 31	100 sps	Passed
Analog Channel 32	100 sps	Passed
Analog Channel 33	100 sps	Passed
Analog Channel 34	100 sps	Some values shows up in Analog Channel 24
Analog Channel 35	100 sps	Passed
Analog Channel 36	100 sps	Passed
Analog Channel 37	100 sps	Passed
Analog Channel 38	100 sps	Passed
Analog Channel 39	100 sps	Passed
Analog Channel 40	100 sps	Passed
Analog Channel 41	100 sps	Passed
Analog Channel 42	100 sps	Passed

Table B-1 continued

Analog Channel 43	100 sps	Passed
Analog Channel 44		Not used
Analog Channel 45		Not used
Analog Channel 46		Not used
Analog Channel 47		Not used
Analog Channel 48		Not used
Analog Channel 49	100 sps	Feed over with Analog Channel 2
Analog Channel 50	100 sps	Values turn up even at Analog Channel 3
Analog Channel 51	100 sps	Some values shows up even at Analog Channel 4
Analog Channel 52	1 ksps	Same values are shows up at Analog Channel 53
Analog Channel 53	1 ksps	Values shows up at Analog Channel 54 instead of Analog Channel 53
Analog Channel 54	1 ksps	Values shows up Analog Channel 21
Analog Channel 55	100 sps	Some values shows up in Analog Channel 14
Analog Channel 56	100 sps	Some values shows up in Analog Channel 15
Analog Channel 57	100 sps	Feed through on Analog Channel 13
Analog Channel 58	100 sps	Same values are observed in Analog Channel 43
Analog Channel 59	100 sps	Feed through with Analog Channel 10
Analog Channel 60	100 sps	Feed through with Analog Channel 11
Analog Channel 61		Not used
Serial Channel 0	115.2 k Baud Rate	Failed the acceptance loop back test as described in user guide of FOXIE-07
Serial Channel 1	19.2 k Baud Rate	Passed
Serial Channel 2	19.2 k Baud Rate	Passed
Serial Channel 3	9600 Baud Rate	Passed
Parallel Channel 0	100 sps	Passed

Table B-1 continued

Parallel Channel 1	100 sps	Passed
Parallel Channel 2	100 sps	Passed
Parallel Channel 3	100 sps	Passed

Appendix-C

Test Results for FOXIE-07

Table C-1 Test Results for FOXIE-07

Channels	Sampling Rate	Notes
Analog Channel 0	100 sps	Passed
Analog Channel 1	100 sps	Passed
Analog Channel 2	100 sps	Passed
Analog Channel 3	100 sps	Passed
Analog Channel 4	100 sps	Passed
Analog Channel 5	100 sps	Passed
Analog Channel 6	100 sps	Passed
Analog Channel 7	100 sps	Passed
Analog Channel 8	100 sps	Passed
Analog Channel 9	100 sps	Passed
Analog Channel 10	100 sps	Passed
Analog Channel 11	100 sps	Passed
Analog Channel 12	100 sps	Passed
Analog Channel 13	100 sps	Passed
Analog Channel 14	100 sps	Passed
Analog Channel 15	100 sps	Passed
Analog Channel 16	2 ksps	Passed
Analog Channel 17	2 ksps	Passed
Analog Channel 18	2 ksps	Passed
Analog Channel 19		Not used

Table C-1 continued

Analog Channel 20	1 ksps	Passed
Analog Channel 21	1 ksps	Passed
Analog Channel 22	1 ksps	Passed
Analog Channel 23	1 ksps	Passed
Analog Channel 24	1 ksps	Passed
Analog Channel 25	100 sps	Passed
Analog Channel 26	100 sps	Passed
Analog Channel 27	100 sps	Passed
Analog Channel 28		Not used
Analog Channel 29		Not used
Analog Channel 30		Not used
Analog Channel 31	100 sps	Passed
Analog Channel 32	100 sps	Passed
Analog Channel 33	100 sps	Passed
Analog Channel 34	100 sps	Passed
Analog Channel 35	100 sps	Passed
Analog Channel 36	100 sps	Passed
Analog Channel 37	100 sps	Passed
Analog Channel 38	100 sps	Passed
Analog Channel 39	100 sps	Passed
Analog Channel 40	100 sps	Passed
Analog Channel 41	100 sps	Passed
Analog Channel 42	100 sps	Passed
Analog Channel 43	100 sps	Passed

Table C-1 continued

Analog Channel 44		Not used
Analog Channel 45		Not used
Analog Channel 46		Not used
Analog Channel 47		Not used
Analog Channel 48		Not used
Analog Channel 49	100 sps	Passed
Analog Channel 50	100 sps	Passed
Analog Channel 51	100 sps	Passed
Analog Channel 52	1 ksps	Passed
Analog Channel 53	1 ksps	Passed
Analog Channel 54	1 ksps	Passed
Analog Channel 55	100 sps	Passed
Analog Channel 56	100 sps	Passed
Analog Channel 57	100 sps	Passed
Analog Channel 58	100 sps	Passed
Analog Channel 59	100 sps	Passed
Analog Channel 60	100 sps	Passed
Analog Channel 61		Not used
Serial Channel 0	115.2 k Baud Rate	Passed
Serial Channel 1	19.2 k Baud Rate	Passed
Serial Channel 2	19.2 k Baud Rate	Passed
Serial Channel 3	9600 Baud Rate	Passed
Parallel Channel 0	100 sps	Passed
Parallel Channel 1	100 sps	Passed

Table C-1 continued

Parallel Channel 2	100 sps	Passed
Parallel Channel 3	100 sps	Passed

Appendix-D

User Guide for FOXIE-07

D-1 FOXIE-07 Specifications and Connectors

This section provides details about all the input- output connectors and their required current and voltage levels. Exceeding recommended levels can damage the FOXIE-07.

Power Input Connector (JP0501) Pin outs:

Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9
+12 V	+15 V	+5 V	+3.3 V	-15 V	GND	GND	GND	SIG GND

12 Volt Input Mode (Opto-Power Jumpers in Place)

	Min	Typ	Max	Units
Voltage Input (Pin 1)	9.1	12.5	15.5	V
Current Draw (Pin 1)	270	230	187	mA
Allowable Ripple		190		mV

Bus Input Mode (Opto-Power Jumpers Removed)

	Min	Type	Max	Units
Voltage (Pin 2)	14.7	15.1	15.3	Volts
Voltage (Pin 3)	4.75	5.05	5.25	Volts
Voltage (Pin 4)	3.1	3.33	3.51	Volts
Voltage (Pin 5)	-14.7	-15.1	-15.3	Volts
Current (Pin 2)		40	60	mA
Current (Pin 3)		140	150	mA
Current (Pin 4)		325	360	mA
Current (Pin 5)		50	60	mA

Parallel Input Connector (JB0501) Pin outs:

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	P0.0	11	P1.2	21	P2.4	31	P3.6
2	P0.1	12	P1.3	22	P2.5	32	P3.7
3	P0.2	13	P1.4	23	P2.6	33	STROBE
4	P0.3	14	P1.5	24	P2.7	34	GND
5	P0.4	15	P1.6	25	P3.0	35	GND
6	P0.5	16	P1.7	26	P3.1	36	GND
7	P0.6	17	P2.0	27	P3.2	37	GND
8	P0.7	18	P2.1	28	P3.3		
9	P1.0	19	P2.2	29	P3.4		
10	P1.1	20	P2.3	30	P3.5		

Parallel Input Connector is a D-SUB 37-pin MALE for FOXIE-07.

P0-31 are LVCMOS logic inputs.

Pin 33 is the LVCOMS STROBE output.

Logic Levels

	Min	Typ	Max	Units
VOL (pin 33)	0.1	0.2	0.3	Volts
IOL (pin 33)	24		48	mA
VOH (pin 33)	2.3	3.1	3.3	Volts
IOH (pin 33)	24		48	mA
VIL (pins 1-32)	0.01	0.8	1.2	Volts
VIH (pins 1-32)	2.1	2.4	3.2	Volts
I_IN (pins 1-32)			10	uA
VTHRS (pins 1-32)		1.85		Volts

VTHRS is the logical threshold voltage

VIL = Voltage Input Low

VIH = Voltage Input High

IOL = Current Output Low (sinking)

IOH = Current Output High (sourcing)

VOH = Voltage Output High

VOL = Voltage Output Low

Analog Connectors (JA0501-02) Pin outs:

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1,2	+/- ACH0	17,18	+/- ACH8	32,33	+/- ACH16	49,50	+/- ACH24
3,4	+/- ACH1	19,20	+/- ACH9	34,35	+/- ACH17	51,52	+/- ACH25
5,6	+/- ACH2	21,42	+/- ACH10	36,37	+/- ACH18	53,54	+/- ACH26
7,8	+/- ACH3	22,23	+/- ACH11	38,39	+/- ACH19	55,56	+/- ACH27
9,10	+/- ACH4	24,25	+/- ACH12	40,41	+/- ACH20	57,58	+/- ACH28
11,12	+/- ACH5	26,27	+/- ACH13	43,44	+/- ACH21	59,60	+/- ACH29
13,14	+/- ACH6	28,29	+/- ACH14	45,46	+/- ACH22	61,62	+/- ACH30
15,16	+/- ACH7	30,31	+/- ACH15	47,48	+/- ACH23		

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1,2	+/- ACH31	17,18	+/- ACH39	32,33	+/- ACH47	49,50	+/- ACH55
3,4	+/- ACH32	19,20	+/- ACH40	34,35	+/- ACH48	51,52	+/- ACH56
5,6	+/- ACH33	21,42	+/- ACH41	36,37	+/- ACH49	53,54	+/- ACH57
7,8	+/- ACH34	22,23	+/- ACH42	38,39	+/- ACH50	55,56	+/- ACH58
9,10	+/- ACH35	24,25	+/- ACH43	40,41	+/- ACH51	57,58	+/- ACH59
11,12	+/- ACH36	26,27	+/- ACH44	43,44	+/- ACH52	59,60	+/- ACH60
13,14	+/- ACH37	28,29	+/- ACH45	45,46	+/- ACH53	61,62	+/- ACH61
15,16	+/- ACH38	30,31	+/- ACH46	47,48	+/- ACH54		

Analog Voltage Ranges

The analog channels are designed for a voltage range of ±10 V. No over-voltage protection or anti-aliasing is provided on the FOXIE-07. Exceeding these ranges will damage

the FOXIE-07 High Speed Digitizer.

Serial Media Connectors (JF0501-08):

The serial inputs are simple one-wire half-duplex fiber optic inputs. Simply connect a 1 mm DNP plastic Fiber-optic core cable to the terminal and screw down the crimp connector on the receiver.

Output and Diagnostic Connector (JB0502):

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	Bi-0-L	11	NRZ-LT	21	TP2	31	ALT6
2	GND	12	RNRZ-LT	22	TP3	32	ALT7
3	Bi-0-D	13	BIT CLK	23	TP4	33	ALT8
4	GND	14	WORD LOAD	24	GND	34	ALT9
5	NRZ-L	15	MINOR CLOCK	25	GND	35	ALT10
6	GND	16	MAJOR CLOCK	26	ALT1	36	GND
7	RNRZ-L	17	RxD	27	ALT2	37	GND
8	GND	18	TxD	28	ALT3		
9	Bi-0-LT	19	GND	29	ALT4		
10	Bi-0-DT	20	TP1	30	ALT5		

Main Outputs

The main outputs (pins 1-8) are AC signals with a total of 3.3 V p-p centered on 1.5 V DC. Bi-0-L and Bi-0-D are the Manchester outputs. NRZ-L is the basic NRZ output and RNRZ-L is the randomized output. Output impedance is 75 ohms and the bandwidth is 17 MHz.

TTL Level Outputs

Pins 9-16 are TTL level outputs. The first four mirror the main outputs with 0-5 V TTL levels. Minor Clock is strobed at the start of each sub-frame, while Major Clock is strobed at the beginning of each frame. Word-Load is strobed at the beginning of each word, while Bit-clock is the bit-rate frequency. These four outputs are provided for diagnostics of the clocks.

RS-232 Connection

A half duplex, 1200 baud signal is provided at the output of the pin (TxD). The waveform is a 600 Hz square wave corresponding to the character "U." This connection should be used for diagnostic purposes only unless a design modification is made.

Test Point Outputs

It is strongly recommended to leave all "TP" and "EXP" pins unconnected unless a design modification has been made to the FOXIE-07 utilizing these pins. Misuse of these pins could damage the FOXIE-07.

Programming Connector

This connector is mapped to an Altera Byte Blaster II or equivalent programmer. Simply connect Pin 33 to pin 1 on the connector for a remote programming interface. See Altera documentation for functions of each pin.

D-2 FOXIE-07 Internal Hardware Structure

Station Identifier Addresses - Each Data Station in the FOXIE-07 encoder has a unique hex address associated with it. The following is a list of active data-stations in the FOXIE-07.

Address	Handle	Type
0000H	Sync Word 0 (SW0)	Sync Word
0001H	Sync Word 1 (SW1)	Sync Word

Address	Handle	Type
0002H	Sync Word 2 (SW2)	Sync Word
0003H	Sync Word 3 (SW3)	Sync Word
0004H	SFID	Sub-frame Identifier
0005H	P0	Parallel Port 0
0006H	P1	Parallel Port 1
0007H	P2	Parallel Port 2
0008H	P3	Parallel Port 3
0015H	S0	Serial Port 0
0016H	S1	Serial Port 1
0017H	S2	Serial Port 2
0018H	S3	Serial Port 3
0019H	S4	Serial Port 4
001AH	S5	Serial Port 5
001BH	S6	Serial Port 6
001CH	S7	Serial Port 7
0020-005FH	A0-63	Analog Channels 0-63
0070-00AFH	SA0-63	Simulated Analog Channel 0-63
0120H	TSA	Time-stamp "A"
0121H	TSB	Time-stamp "B"

Special Function Registers

The FOXIE-07 Special Function Registers (SFR) configures and controls the FOXIE-07 encoder hardware within the Cyclone FPGA. The following is a list of the SFR's and their functions. The HEX addresses refer to the external bus address used to access (write only) each register from the MSP430 microprocessor. This process is automated by the TACOSMATRIX software.

Bit Rate Register (4000H)

This register sets the FOXIE-07 bit rate. There are 16 possible bit rates to choose form –

Register Value in Hex	Bit Rate
0	25 kbps
1	50 kbps
2	100 kbps
3	200 kbps
4	250 kbps
5	400 kbps
6	640 kbps
7	800 kbps
8	1.0 Mbps
9	1.2 Mbps
A	1.6 Mbps
B	2.0 Mbps
C	2.4 Mbps
D	3.2 Mbps
E	4.0 Mbps
F	4.8 Mbps

Bits per Word Register (4001H)

This register is used to select the length of the word for the telemetry data matrix –

Register Value in Hex	**Word Size**
0	10 bit words
1	12 bit words
2	14 bit words
3	16 bit words

Minor-frame and Frame Size Registers (4002-4003H)

These registers take the user's hex input value, add four to it and use it to represent the maximum minor-frame and frame size in the encoder's framing engine. The four offset is automatically compensated for by the TACOSMATRIX utility. The maximum size is 64

x 64 (as limited by the PCM matrix memory – 4096 x 16 bits). FOXIE-07 had a 32 x 32 matrix. Hexadecimal value of the Minor-frame and Frame should be entered into these registers.

Sync-word Pattern Registers (400C-400FH)

Each of these 16-bit registers holds the sync word pattern that can be accessed through the stations SW0-3. The 16-bit pattern is MSB justified. In the case of encoder word sizes less than 16 bits, only the MSB's are used.

Serial Baud Rate Registers (4004-400BH)

Each of these registers sets the serial baud rate for the corresponding serial channel (0-7) by programming the baud-generator. For example, to set the baud rate of serial channel S0, the special function register S0 in the data matrix can be populated with any of the 10 possible baud rate values. The table below shows the hexadecimal value of the possible baud rates.

Value in Hexadecimal	Baud Rate
0	1200 bps
1	2400 bps
2	9600 bps
3	19.2 kbps
4	28.8 kbps
5	38.4 kbps
6	57.6 kbps
7	115.2 kbps
8	230.4 kbps
9	460.8 kbps

PCM Matrix Memory (0000-3FFFH)

The PCM matrix stores sequentially the stations ID's to be encoded and sampled in a frame.

The maximum frame size is 4096 words. The memory should never be written without asserting the TMHO_N pin and thereby resetting the encoder. All operations with the PCM matrix memory are automated by the TACOSMATRIX utility and the MSP430.

D-3 Assembly and Configuration

The following steps have to be taken to integrate FOXIE-07 into a rocket payload –

- Burn the data matrix and special functions registers from the TACOSMATRIX utility to the AT25256A EEPROM. The data can be burned into the EEPROM using EEPROM writer from EETools. Place the EEPROM in the socket on the Core Board.
- Prepare the FOXIE-07 mounting spot, and insert 4, 4-40 standoffs with the male end up.
- Loosely secure the standoffs to the deck-plate or mounting base with 4-40 screws.
- Place the FOXIE-07 Serial media board on the 4 standoffs. Align the media board in the desired direction before placement.
- Screw on 4 more 4-40 1/2" standoffs on top of the serial media board. Secure firmly add the FOXIE-07 parallel board and repeat the standoff process. Repeat the same process for the Core Board and the Analog Board.
- The FOXIE-07 is now ready to be integrated into the payload.

D-4 FOXIE-07 Firmware and Hardware Files

A CD containing all the firmware, software and hardware files is provided to ASGP for future modifications and developments of FOXIE.